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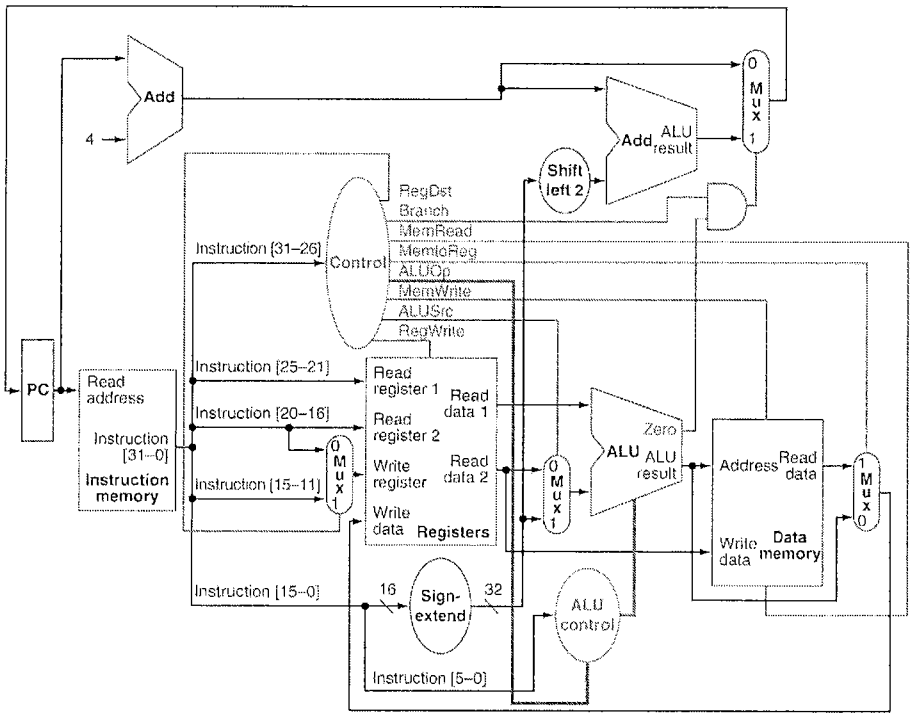
一、[15%] Below is one implementation of the datapath of the simple MIPS processor. Suppose that all instructions have the same instruction fetch and decode steps. The critical paths for the different instruction types that need to be considered are: R-format, Load-word, and Store-word.



The operation times for the major functional components for this machine are listed as follows:

Component	Latency (ns)
ALU	10
Adder	8
ALU Control Unit	2
Shifter	3
Control Unit/ROM	4
Sign / zero extender	3
2:1 MUX	2
Memory (read/write) (instruction or data)	15
PC Register (read action)	1
PC Register (write action)	1
Register file (read action)	7
Register file (write action)	5
Logic (1 or more levels of gates)	1

(a) [10%] Please indicate the components that determine the path delay for each type of R-format, Load-word, and Store-word instructions, respectively, in the order that the critical path occurs.

(b) [5%] For this MIPS processor, what will the resultant clock cycle time be? And what frequency will the machine run?

二、[10%] The following table shows the number of instructions for a typical program:

Arithmetic	Store	Load	Branch	Total
500	50	100	50	700

(a) [5%] Assuming that Load instruction takes 5 cycles, Arithmetic and Store 4 cycles and Branch 3 cycles, what is the execution time of the program running in 2 GHz processor? Find the CPI for the program?

(b) [5%] If the number of load instructions can be reduced by one-half, what is the speed-up and CPI.

三、[10%]

(a) [5%] Given by a floating-point number $24A60004_{(hex)}$ that is represented by IEEE 754 standard. What decimal number is it?

(b) [5%] Write down the binary representation of the decimal number -1609.5, assuming the IEEE 754 double precision format.

四、[15%] For a direct-mapped cache design with 32-bit address [31—0], the following bits of the address are used to access the cache:

	Tag field	Index field	Offset field
Case I	[31—10]	[9—4]	[3—0]
Case II	[31—12]	[11—5]	[4—0]

(a) [4%] What is the block size (in words) of each case?

(b) [3%] For each case, what is the ratio between total bits required for such a cache implementation over the data storage bits?

Starting from power on, the following byte-addressed cache references are recorded:

address	0	4	16	132	232	160	1024	30	140	3100	180	2180

(c) [4%] For each case, how many blocks are replaced?

(d) [4%] For each case, what is the hit ratio?

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五、 [17%] Some recursive procedures can be implemented iteratively without using the recursion. Given the following C program segment, the converted MIPS assembly codes are shown as below. Assume that arguments n and acc locate in $a0 and $a1.

```
int prod(int n, int acc) {
    if (n > 0)
        return prod(n-2,n*acc);
    else
        return acc;
    }
```

(a) [7%] Please fill in the blanks (I) to (VII) to complete this assembly codes.

```
Prod: slti $t0, $a0, __(I)__
      bne  $t0, $zero, Exit
      mult __(II)__, $a0, __(III)__
      addi __(IV)__ , $a0, -2
      j    Prod
Exit: add  __(V)__, __(VI)__ ,$zero
      jr   __(VII)__
```

	op	rs	rt	rd	sht	funct
48000(dec)						
48004(dec)	5	8	0	(VIII)		
48008(dec)						
48012(dec)	8	4		(IX)		
48016(dec)	2	(X)				
48020(dec)						
48024(dec)						

(b) [6%] Parts of the corresponding machine language instructions are also given. Please fill the blanks (VIII), (IX), and (X) in decimal.

(c) [4%] Let the initial values of $a0 and $a1 are $8_{(hex)}$ and $7_{(hex)}$, respectively. How many times is the instruction "j Prod" executed before the completion of the program? What is the value of $v0 when the last instruction is executed? Please express in decimal.

六、 [25%] Assume that an engineer is asked to design a new pipeline processor, which is based on the MIPS ISA, to accelerate neural network computations. Thus, he plans to add a new instruction "macc", which combines multiplication and addition in a single instruction. Its operation example is given as follows.

```
macc $s0,$s1,$s2     =     mult  $t0,$s1,$s2
                           add   $s0,$s0,$t0
```

Assume that in a conventional 5-stage pipelined MIPS ISA design, the individual pipeline stages are named as IF, ID, EX, MEM, and WB. The latencies of five stages are given as 120ps, 100ps, 170ps, 200ps, 120ps. In the new processor, due to the revision of ID and EX to support the new instruction, the latencies of ID and EX stages become 120ps and 240ps. Now, let's examine the effect of his design by the following C codes and assembly codes given that variable NodeOut and LENG are in register $s3 and $s4. The bases of arrays Weight and InMap are in $s0 and $s1.

```
for (i = 0; i <LENG; i += 1)
    NodeOut=NodeOut+Weight[i]*InMap[i];
```

1		add	$t1, $zero, $zero
2	LOOP:	sll	$t2, $t1, 2
3		add	$t3, $s0, $t2
4		add	$t2, $s1, $t2
5		lw	$t4, 0($t3)
6		lw	$t5, 0($t2)
7		mult	$t5, $t4, $t5
8		add	$s3, $t5, $s3
9		addi	$t1, $t1, 1
10		slt	$t3, $t1, $s4
11		beq	$t3, $zero, EXIT
12		j	LOOP
13	EXIT:		

(a) [6%] Consider only the effect inside the loop. If there is no forwarding or hazard detection, please insert `nops` and rewrite the assembly to ensure correct execution for the assembly codes from line 2 and line 8 given the conventional MIPS ISA.

(b) [4%] From (a), what is the processing time for completing these 7 instructions given the maximum operating frequency?

(c) [6%] Let the new instruction "`macc`" replace line 7 and line 8 of the above assembly codes. If there is no forwarding or hazard detection, please insert `nops` and rewrite the assembly to ensure correct execution for the assembly codes on the new pipeline processor.

(d) [4%] From (c), what is the processing time for completing these 6 instructions given the maximum operating frequency?

(e) [5%] Please comment according to (b) and (d). (You will get points only when answers in (b) and (d) are correct.)

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七、[8%]

(a) [4%] If we want to use multi-processors to speedup the computation of an inner product of two vectors of size 100×1. Let the execution time of a single processor for this inner-product operation of two vectors of size 100×1 is t. Assume that 90% instructions associated with arithmetic operations can be processed in parallel, what is the execution time and speed-up with 10 processors?

(b) [4%] From (a), given that the vector size become 400×1 and the processing time of a single processor for this inner-product operation is $3.8t$, if we want to achieve more than $8\times$ speed-up, at least how many processors should we use? What is the execution time?