

國立中央大學 107 學年度碩士班考試入學試題

所別： 資工類

共 2 頁 第 1 頁

科目： 作業系統與計算機組織

本科考試禁用計算器

*請在答案卷(卡)內作答

多選題 (每題五分, 每一選項單獨計分, 答錯倒扣一分)

1. Choose the correct statements from the multiple choices regarding the fork() system call.
 - (A) The new process created by the fork() system call consists of a copy of the address space of the original process.
 - (B) The copy-on-write (COW) technique can be used to reduce copying memory in fork().
 - (C) The return code for the fork() is zero for the original process.
 - (D) The exec() system call loads a binary file into memory and starts its execution.
 - (E) None of the above.
2. Choose the correct statements from the multiple choices regarding atomic transactions.
 - (A) An un-interruptible unit is known as atomic.
 - (B) Incrementing an integer value can always be performed atomically.
 - (C) The TestAndSet instruction is executed atomically.
 - (D) The mutual exclusion of critical sections ensures that the critical sections are executed atomically.
 - (E) None of the above.
3. Choose the correct statements from the multiple choices regarding networking.
 - (A) Because of the 32-bit IPv4 address space, it is impossible for more than 2^{32} computers to communicate over the internet.
 - (B) You can use a socket to communicate between two processes on the same machine.
 - (C) ICMP protocol is used to find the hardware address of a local device.
 - (D) If the sender is a host and it wants to send a packet to another host on another network, the logical address that must be mapped to a physical address is the destination IP address in the header.
 - (E) None of the above.
4. Choose the correct statements from the multiple choices.
 - (A) Dirty bit is used to indicate that the associated page has been modified.
 - (B) The scheme of modify bit can reduce the time required to service a page fault.

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- (C) The operating system sets the valid-invalid bit for each page to allow or disallow access to the page.
- (D) When the valid-invalid bit is set to valid, the associated page is the system's physical address space.
- (E) None of the above.
5. Choose the correct statements from the multiple choices.
- (A) A process cannot be run by an operating system if some of its pages are swapped out.
- (B) Dynamic loading does not require special support from the operating system.
- (C) Spinlocks are wasteful if locks are held for only short times.
- (D) Spinlocks avoid the overhead from context switches.
- (E) None of the above.
6. Most systems allow programs to allocate more memory to its address space during execution. Data allocated in the heap segments of programs is an example of such allocated memory. What is required to support dynamic memory allocation in the following schemes:
- (A) contiguous-memory allocation.
- (B) pure segmentation.
- (C) pure paging.
- (D) paged segmentation.
- (E) none
7. Consider a demand-paging system with the following time-measured utilizations: CPU utilization 20% , Paging disk 97.7%, Other I/O devices 5%
- Which (if any) of the following will (probably) improve CPU utilization?
- (A) Install a faster CPU.
- (B) Install a bigger paging disk.
- (C) Increase the degree of multiprogramming.
- (D) Decrease the degree of multiprogramming.
- (E) Install more main memory.

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8. Which of the following programming techniques and structures are good for a demand-paged environment ?
- (A) Stack
 - (B) Hashed symbol table
 - (C) Sequential search
 - (D) Binary search
 - (E) pure code
9. What are the purpose of the separation of mechanism and policy:
- (A) Easy to programming
 - (B) Systems are easy to modify
 - (C) Flexibility to suit its needs
 - (D) Increasing utilization
 - (E) Quick and fast system response
10. Some computer systems do not provide a privileged mode of operation in hardware. To construct a secure operating system for these computer systems, an OS for a machine of this type would need to remain in control at all times. This is could be accomplished by the following methods:
- (A) co-execution with co-processor to execute all programs.
 - (B) networked server support to execute programs.
 - (C) all programs be written in high-level languages so that all object code is compiler produced and checked.
 - (D) cluster computing in database cloud system.
 - (E) software interpretation of all user programs.
11. Which of the following expressions, E1 and E2, are equivalent?
- (A) $E1(A,B,C)=A'BC+AB'C+ABC'+ABC$
 $E2(A,B,C)=(A+B+C)(A+B+C')(A+B'+C)(A'+B+C)$
 - (B) $E1(A,B,C)=BC+AB'C+AB'C'+A'BC'$
 $E2(A,B,C)=AB'+A'B+ABC$
 - (C) $E1(A,B,C,D)=AC+BC+A'B'C+B'C'D'$
 $E2(A,B,C,D)=C+B'D'$
 - (D) $E1(A,B,C,D)=\sum(0,1,4,5,6,7,8,9,12,13,14,15)$ (Note: \sum : sum of minterms.)

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$$E2(A,B,C,D)=C'+BD$$

(E) $E1(A,B,C,D)=\prod(3,4,6,7,11,12,14,15)$ (Note: \prod : product of maxterms.)

$$E2(A,B,C,D)=B'D'+C'D$$

12. Assume the individual stages of the datapath have the following latencies:

- IF: 300 ps
- ID: 150 ps
- EX: 250 ps
- MEM: 350 ps
- WB: 200 ps

Which of the following statements are true?

- (A) If the processor is non-pipelined, the cycle time is 350 ps
- (B) If the processor is pipelined, the cycle time is 1250 ps
- (C) If the processor is non-pipelined, the total latency of an LW instruction is 1250 ps
- (D) If the processor is pipelined, the total latency of an LW instruction is 1750 ps
- (E) None of above

13. Consider the following MIPS instruction sequence with a pipelined processor without forwarding:

OR R1, R2, R3 # I1

AND R2, R1, R4 # I2

XOR R1, R1, R2 # I3

Assume the cycle time is 300 ps. Which of the following statements are true?

- (A) A RAW hazard occurs on R1 from I1 to I2 and from I1 to I3
- (B) A RAW hazard occurs on R2 from I1 to I2
- (C) We need to add two NOP instructions to eliminate the hazards
- (D) The total execution time is 2700 ps
- (E) None of above

14. Why can the pipeline enhance the throughput?

- (A) Because pipeline reduces the clock rate
- (B) Because pipeline enables all stages are used in parallel
- (C) Because pipeline reduces the instruction count

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- (D) Because pipeline reduces the response time of an instruction
(E) None of above

15. What is correct about branch prediction?

- (A) Branch prediction helps prevent data hazard
(B) Static branch prediction predicts the branches at runtime using runtime information
(C) The compiler mainly decides dynamic branch prediction
(D) Static branch prediction usually outperforms dynamic branch prediction
(E) None of above

單選題 (每題五分, 答錯倒扣 2 分)

16. A 2-way set-associative 128KB cache addressed by a 32-bit virtual address has the block size equal to 64 bytes. The tag field of address has "A" bits. The CPU accesses the following memory sequence after the system is reset.

0x1D34B2BE

0x1D34B2CF

0x1D34B286

0x1D34B2E8

0x1D38B2D9

0x1D38C2DA

0x1D3DB2E7

0x1D34B2E6

Assume that the strategy of LRU is adopted. The number of cache misses is "B".

What is $\text{mod}((A+B), 5)$? (Note: $\text{mod}(\cdot)$ is the modulo operation.)

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

17. Two computers, Pineapple(P) and Watermelon(W), adopt the same ISA. The clock rate of CPU in P is 2.4GHz and the clock rate of CPU in W is 2GHz. A program is compiled to run on these two machines. The compiler LP is used for the computer P and the compiler LW is used for the computer W. The numbers of resultant machine instructions of this program after compilation on P and W are 17.6 million and 1.2

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million, respectively. Assume that there are three instruction classes, IA, IB and IC, and their CPI on two machines are shown below:

Instruction Class	CPI for P	CPI for W
IA	2	3
IB	3	2
IC	4	5

The instruction mix is as follows,

Instruction Class	Compiled by LP	Compiled by LW
IA	30%	40%
IB	40%	40%
IC	30%	20%

Calculate the execution time, TP, for using LP on P, and the execution time, TW,

for using LW on W. Then, what is $\text{mod}(\text{round}(\frac{TW}{TP} \times 110), 5)$?

(Note: round(X) is to find the closest integer of X.)

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

18. Suppose there are 1000 memory references. 100 misses happen in L1 cache, 20 misses happen in L2 cache, and 5 misses happen in L3 cache. Assume that the miss penalty of L3 cache (to the main memory) is 100 clock cycles, the hit time of L3 cache is 10 clock cycles, the hit time of L2 cache is 5 clock cycles, and the hit time of L1 cache is 1 clock cycle. The average memory access time is "T" clock cycles. What is $\text{mod}(\text{round}(T \times 13), 5)$?

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

19. In 32-bit single-precision IEEE754 floating-point numbers, the largest normalized number is "K" and the largest denormalized number is "J". If the number of "0" bits in "K" is "ZK" and the number of "0" bits in "J" is "ZJ". Then, what is $\text{mod}(ZK+ZJ, 5)$?

(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

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20. A program has 4 billion instructions. If the instructions are executed by a pipelined CPU with 4 stages and clock rate 2 GHz, what is the approximated execution time (assuming that on average each instruction causes 1.2 stall cycles)?
(A) 2 seconds (B) 2.4 seconds (C) 4.4 seconds (D) 4.8 seconds (E) 5.2 seconds

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