

參考用

I. 多選題，每題 5 分

1. Which of the following statement(s) should be true?

- (a) There are more addressing modes in CISC than in RISC.
- (b) Microprogramming is usually used in CISC since this kind of control can be executed faster.
- (c) Horizontal microinstructions are executed faster than Vertical microinstructions.
- (d) Using ROM in the control designs can usually save the space or cost, when compared with PLA.
- (e) None of the above is true.

2. About the performance analysis, which of the following statement(s) should be true?

- (a) Assume that a C program is compiled into 1000 machine instructions, which are related to the size of the executable file. Then, the average execution time is usually equal to multiplying 1000 (instructions) by its average CPI and the clock cycle time.
- (b) In evaluating the performance by using the benchmark tests, we usually use the geometric mean to calculate the average value among various test results.
- (c) MIPS is not a reliable metric since it provides the wrong results when we compare the performances of a compiled program running on two machines with the same instruction set architecture.
- (d) It is usually a preferred approach to consider only one of the three factors: clock rate, CPI or the instruction count, and then try to improve it to decrease the execution time. That is called a divide-and-conquer methodology.
- (e) None of the above is true.

3. About the memory hierarchy, which of the following statement(s) should be true?

- (a) A page fault happens if a page that is not in the physical memory is accessed.
- (b) TLB is a data cache of main memory.
- (c) Adding a secondary cache can help to reduce the miss rate.
- (d) We can always increase the size of cache to improve the cache performance.
- (e) None of the above is true.

4. Peterson's solution is a software-based solution to the critical-section problem. For two processes accessing a shared variable, Peterson's solution provides:

- (a) Hold and wait (b) Progress (c) Mutual exclusion (d) Circular wait (e) None of the above

注意：背面有試題

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5. Choose the correct statements from the multiple choices regarding the process management.
- (a) The fork() system call is able to create a new process.
  - (b) The fork() system call is able to determine how much sharing is to take place between the parent and child tasks.
  - (c) Linux provides the ability to create threads using the clone() system call.
  - (d) A new program is run after a call to exec().
  - (e) None of the above
6. Choose the correct statements from the multiple choices regarding virtualization.
- (a) The guest operating system runs on top of host operation system.
  - (b) In para-virtualization, a guest operating system runs unmodified on a hypervisor.
  - (c) Para-virtualization presents the guest with a system that is identical to the guest's preferred system.
  - (d) Both of virtual user mode and virtual kernel mode run in a physical user mode on the host.
  - (e) None of the above
7. Choose the correct statements from the multiple choices regarding network protocols.
- (a) IPv6 does not define broadcasting.
  - (b) IPv6 supports anycasting.
  - (c) ARP protocol is used for resolution of network layer addresses into link layer addresses.
  - (d) DNS converts domain names to IP addresses.
  - (e) None of the above
8. What are the advantages of register-register ALU instruction type compared with register-memory ALU instruction type and memory-memory ALU instruction type?
- (a) Data can be accessed without loading first.
  - (b) Fixed-length
  - (c) Simple code-generation
  - (d) Instructions take similar Clock Cycle per Instruction (CPI) to execute.
  - (e) Large variation in instruction size
9. What are the properties critical to program correctness that are normally preserved by control dependency?
- (a) Temporal locality
  - (b) Spatial locality
  - (c) Exception behavior
  - (d) Data flow

注：背面有試題

參考用

(e) None of the above

10. What of the following statements are true?

- (a) If some combination of instructions cannot be accommodated because of resource conflicts, the machine is said to have a structural hazard.
- (b) The potential overlap among instructions is called Instruction-Level Parallelism.
- (c) If there exists a loop-carried dependence, it is not possible to transform the code and unroll the loop to make iterations be executed in parallel.
- (d) Hazards usually have smaller impact on longer pipelines.
- (e) For a cache with write through strategy, read misses cannot result in writes.

11. Select the items which are needed to be supported by the operating system for handheld devices.

- (a) Batch programming
- (b) Virtual memory
- (c) Time sharing
- (d) Interrupt driving I/O
- (e) RAID

12. Which of the following components of program state are shared across threads in a multithreaded process?

- (a) Register values
- (b) Heap memory
- (c) Global variables
- (d) Stack memory
- (e) Local variables

II. 單選題，每題 5 分

13. Assume that a computer uses 32-bit addressing and has a 1MB cache with the block size equal to 32 bytes. The size of the Tag field in the address for a direct mapped cache is L. The size of the Tag field in the address for an 8 way set associative cache is M. The size of the Tag field in the address for a fully associative cache is N.  $L+M+N=K$  and

- (a)  $K < 50$
- (b)  $50 \leq K < 55$
- (c)  $55 \leq K < 60$
- (d)  $60 \leq K < 65$
- (e)  $65 \leq K$

注意：背面有試題

參考用

14. A cache with 64 blocks and a block size of 32 bytes. The byte address 2473537 maps to the block number  $K$  ( $0 \leq K < 64$ ).  $K \bmod 5$  equals to?

- (a) 0
- (b) 1
- (c) 2
- (d) 3
- (e) 4.

15. The following table shows the information about a machine executing instructions. There are 5 classes of instructions, each of which takes 3~5 steps.

Instruction Class	Fetch	Register Read	ALU	Memory access	Register Write
Load Word (LW)	2ns	1ns	2ns	3ns	1ns
Store Word (SW)	2ns	1ns	2ns	3ns	
R-Format (R)	2ns	1ns	2ns		1ns
Branch (B)	2ns	1ns	2ns		
Jump (J)	2ns	1ns	2ns		

For a certain program, 25% of the instructions are LW, 10% are SW, 45% are R, 15% are B, 5% are J. Consider the following three cases: (i) If there is no pipelining, the average time required for executing one instruction is  $L$  (ns). (ii) If a 5-stage pipeline is adopted, the average time required for executing one instruction in the ideal case is  $M$  (ns). (iii) Assume that the destinations of Branch (B) and Jump (J) will not be known until the end of the ALU stage. If every B or J instruction incurs two pipeline bubbles, the average time required for executing one instruction is  $N$  (ns).  $L+M+N=K$ . Then (a)  $K < 13$  (b)  $13 \leq K < 14$  (c)  $14 \leq K < 15$  (d)  $15 \leq K < 16$  (e)  $16 \leq K$ .

16. Which threading model is supported by the Linux operating system?

- (a) one-to-many
- (b) many-to-one
- (c) one-to-one
- (d) many-to-many
- (e) none of the above

17. Suppose that there is a machine with 32-bit addresses and a two-level page table. Note that the first 10 bits of an address is an index into the first level page table and the next 10 bits are an index into a second level page table. The page tables are stored in memory and each entry in the page tables is 4 bytes. Suppose the space allocated to a specific process is 64 Mbytes. How many pages are occupied by this process?

注意：背面有試題

參考用

- (a)  $2^{26}$  pages
- (b)  $2^{14}$  pages
- (c)  $2^{12}$  pages
- (d)  $2^{10}$  pages
- (e) None of the above

18. (Continued from the previous question.) How much space is occupied in memory by the page tables for the specific process?

- (a) 68 kbytes
- (b) 64 kbytes
- (c) 16 kbytes
- (d) 4 kbytes
- (e) None of the above

19. Assume that an un-pipelined machine has 9ns clock cycles. The machine uses four cycles for ALU operations, four cycles for branches, and five cycles for memory operations. The relative frequencies of these operations are 30%, 20%, and 50%, respectively. Suppose that pipelining the machines adds 1ns of overhead to the clock cycle time. Assume that the ideal CPI is one. Ignore any other impact.

What is the average clock cycle per instruction (CPI) of the un-pipelined machine?

- (a) 5.5
- (b) 4
- (c) 3.5
- (d) 4.5
- (e) 5

20. (Continued from the previous question.) What is the speedup in the instruction execution rate gained from pipelining the machine?

- (a) 4.05
- (b) 4.75
- (c) 5.15
- (d) 5.85
- (e) 6.28

