國立中央大學97學年度碩士班考試入學試題卷

所別：電機工程學系碩士班 電子組、固態組　科目：電子學　共 2 頁 第 1 頁
系統與生醫組、電波組　＊請在試卷答案卷（卡）內作答

參考用

1. 簡答題 (18 分)

Consider the BJT circuits in Fig. 1,

1-1 Please specify the corresponding configuration for each circuit (common-emitter, common-base, or emitter-follower?) (6 分)

1-2 Which R_{in} is the largest? Why? Assume that each BJT has the same $\beta_F = 100$, $V_{BE(on)} = V_{EB(on)} = 0.7$ V. (6 分)

1-3 Which circuit has a voltage gain always less than unity ($A_v \equiv |v_o/v_{sig}| < 1$)? Why? (6 分)

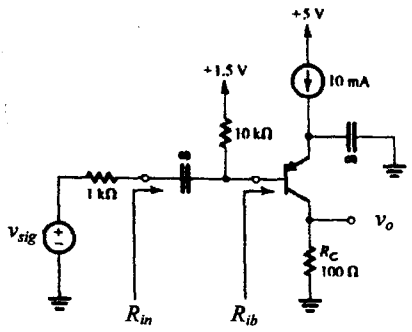


Fig. 1(a)

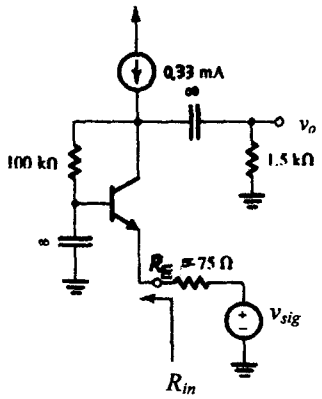


Fig. 1(b)

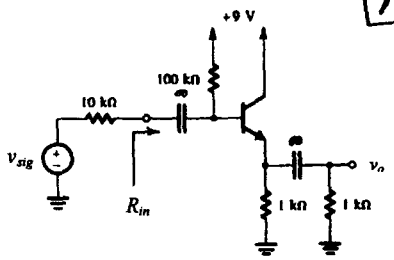


Fig. 1(c)

Fig. 1

2. 計算題 (15 分)

Consider a common-source MOSFET amplifier in Fig. 2. The transistor has $\mu_n C_{ox}(W/L) = 0.25$ mA/V^2, $V_t = 1.5$ V, $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

2-1 Find R_{in} and v_o/v_i. (10 分)

2-2 Find the largest allowable input signal to keep the MOSFET in saturation at all times. (5 分)

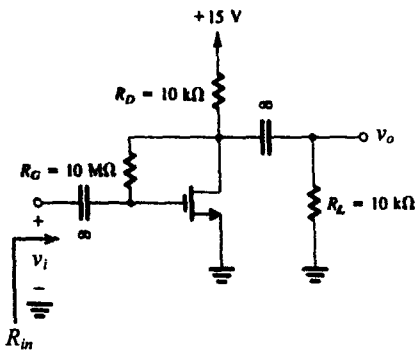


Fig. 2

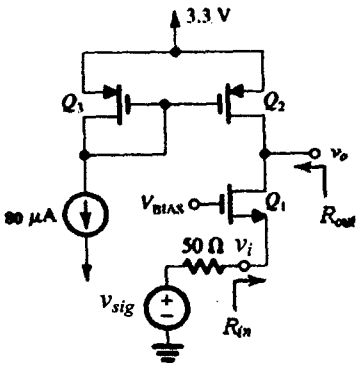


Fig. 3

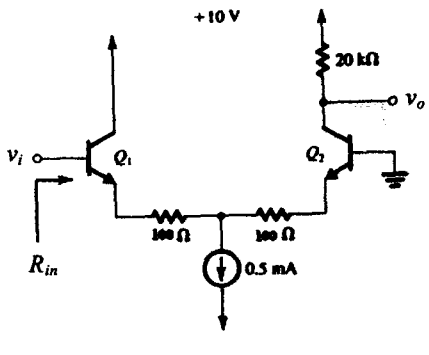


Fig. 4

3. 計算題 (15 分)

Figure 3 shows a CMOS common-gate amplifier with active-loaded, Q_2 and Q_3 are matched, $\mu_n C_{ox}(W/L) = \mu_p C_{ox}(W/L) = 4$ mA/V^2, and all transistors have $|V_t| = 0.8$ V, $|V_A| = 16$ V, and the bias current $I = 80$ μA. Transistor Q_1 has $\chi = 0.25$ for body transconductance g_{mb}. The v_{sig} is a small sinusoidal signal with no dc component.

3-1 Find the values of g_{m1} and g_{mb1}. (5 分)

3-2 Find the value of R_{in}. (5 分)

3-3 Calculate the voltage gain v_o/v_i. (5 分)

4. 計算題 (10 分)

Find the values of the voltage gain v_o/v_i and the input resistance R_{in} of the amplifier shown in Fig. 4 assuming $\beta = 100$ and $V_T = 25$ mV. (10 分)

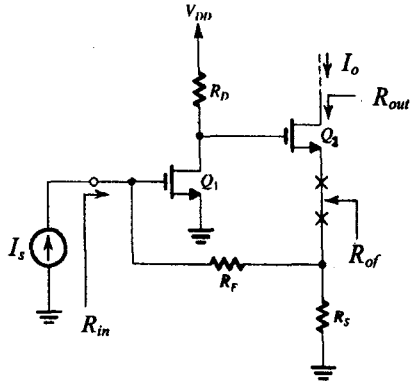
注：背面有試題

5. 選擇題與計算題 (12 分)

Figure 5 shows a feedback amplifier which design parameters are listed as follows, $g_{m1} = g_{m2} = 5$ mA/V, $R_D = R_S = 10$ kΩ, and $R_F = 90$ kΩ. Neglect r_o and body effect.

5-1 Identify the feedback topology to be used. (A) Shunt-Series, (B) Series-Series, (C) Shunt-Shunt, (D) Series-Shunt. (3 分)

5-2 Find the overall gain I_o/I_s. (9 分)



參考用

Fig. 5

6. 作圖題 (5 分)

Sketch a CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

7. 問答題 (5 分)

As shown in Fig. 6, the Content Addressable Memory (CAM) cell is implemented by an SRAM cell with the Tag-Compare Portion. During the precharge phase, the match line (ML) is charged to V_{DD}. Find the final comparison result of the ML when the logic value of (n1, DL) = (1, 1).

8. 問答題 (10 分)

As shown in Fig. 7, which type of logic gate does the circuit implement? Sketch the output waveform of the node Q2.

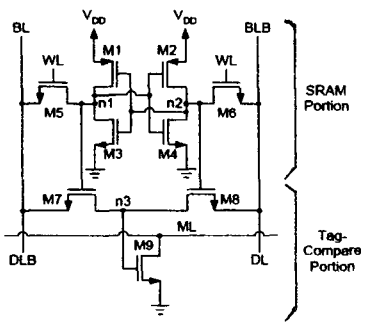


Fig. 6

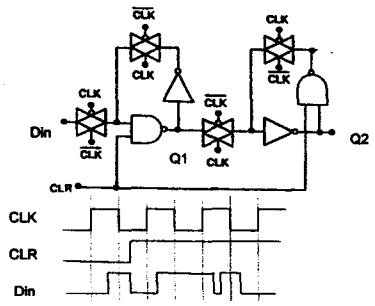


Fig. 7

9. 計算題 (10 分)

A CMOS Inverter with an additional 0.1 pF capacitance load, the design parameters of this CMOS Inverter are listed as following: $(W/L)_n = 10$, $(W/L)_p = 20$, $\mu_n C_{ox} = 2\mu_p C_{ox} = 0.2$ mA/V^2, $V_{tn} = |V_{tp}| = 1$V, $V_{DD} = 5$ V. Assume the gate-drain overlap capacitance and the drain-body capacitance are zero.

9-1 Find the propagation delay t_{PHL}. (5 分)

9-2 Find the dynamic power dissipation when clocked at 50 MHz. (5 分)

注意：背面有試題