國立中央大學94學年度碩士班考試入學試題卷　共 2 頁 第 1 頁

所別：電機工程學系碩士班 乙丙丁組　科目：電子學

1. 選擇與簡答題(10 分, 答對每小題得 2 分)

Consider three cases for pn junctions: (A) $N_D = 10^{20}$ cm^{-3}, $N_A = 10^{19}$ cm^{-3}, (B) $N_D = 10^{19}$ cm^{-3}, $N_A = 10^{17}$ cm^{-3}, and (C) $N_D = 10^{18}$ cm^{-3}, $N_A = 10^{15}$ cm^{-3},

1-1 Which pn junction has the largest junction capacitance as the bias voltage is fixed?

1-2 Which pn junction has the largest reverse breakdown voltage?

1-3 Consider a circuit with two pn diodes as shown in Fig. 1. Under which bias condition, this circuit will behave like a BJT?
(A) $V_{BE} > 0$ and $V_{BC} > 0$ (B) $V_{BE} > 0$ and $V_{BC} < 0$ (C) $V_{BE} < 0$ and $V_{BC} > 0$ (D) None.

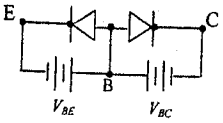

Fig. 1

1-4 Which of the following statement is true? (A) a common-gate amplifier has an infinite input resistance, (B) a common-base amplifier's current gain $|A_i|$ is larger than 1, (C) an emitter follower has an infinite output resistance, and (D) a common-emitter amplifier can have a voltage gain >1 and a current gain >1 simultaneously.

1-5 In a BJT amplifier, why is the emitter-base capacitance (Cπ) usually larger than the collector-base capacitance (Cμ)?

2. 選擇題(14 分)

Consider the circuits (a), (b), (c), and (d) shown in Fig.2, assume that every transistor is biased in the forward-active mode and has the same $\beta_F = 100$, $V_{BE(on)} = 0.7$ V, and $V_A = \infty$. If the current sources I_1, I_2, I_3, and I_4 are adjusted such that each Q_1 transistor has the same dc collector current and hence, the same small-signal parameters.

2-1 Consider the input resistance R_i, (A) which circuit has the largest input resistance?(3 分) (B) Which has the lowest input resistance? (4 分)

2-2 Consider the voltage gain $A_v = |V_{out}/V_{in}|$, (A)which circuit has the largest voltage gain?(3 分) (B))Which has the lowest voltage gain?(4 分)

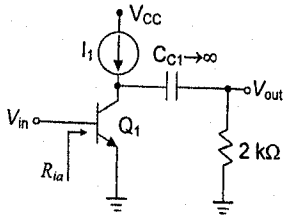

Fig. 2(a)

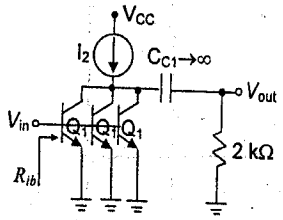

Fig. 2(b)

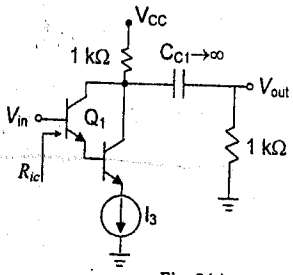

Fig. 2(c)

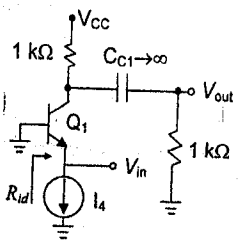

Fig. 2(d)

3. 選擇題(20 分)

For the cascode amplifier as shown in Fig. 3, let Q_1 and Q_2 be identical with $V_t = 0.6$ V, $\mu_n C_{ox} = 160$ μA/V^2, $\lambda = 0.05$ V^{-1}, $\chi = 0.2$, W/L = 100, and $V_{OV} = 0.2$ V.

3-1 (4 分) What must the bias current I can be ? (A) 32 μA, (B) 54 μA, (C) 108 μA, (D) 160 μA, (E) 320 μA.

3-2 (4 分) Find the open circuit voltage gain A_{V0}. (A) 200 V/V, (B) 241 V/V, (C) 4820 V/V, (D) 48200 V/V, (E) 441 V/V.

3-3 (4 分) Calculate the value of the effective short-circuit transconductance, Gm, of the cascode amplifier. (A) 3.2 mA/V, (B) 1.6 mA/V, (C) 6.4 mA/V, (D) 8.0 mA/V, (E) 9.6 mA/V.

3-4 (4 分) Find the output resistance R_{out} of the amplifier (A) 62.5 kΩ, (B) 125 kΩ, (C) 320 kΩ, (D) 2.4 MΩ, (E) 15.125 MΩ.

3-5 (4 分)Ignoring the small signal swing at the input and at the drain of Q_1, find the lowest value that V_{BIAS} should have in order to operate Q_1 and Q_2 in saturation. (A) 0.6 V, (B) 1.0 V, (C) 1.25 V, (D) 1.8 V, (E) 2.2 V.

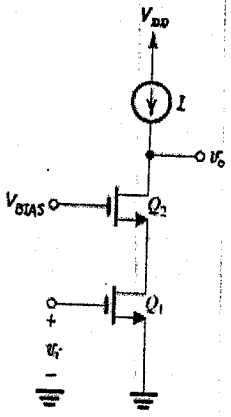

Fig. 3 The MOS cascode amplifier.

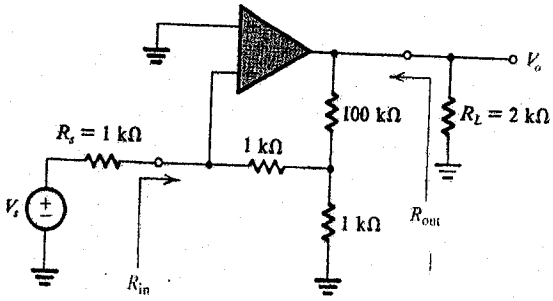

Fig. 4 Circuit for Problem 4

(0,1C)

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4. 選擇題(20 分)

A feedback circuit is shown in Fig. 4, the OP amp has open-loop gain $\mu = 10^4$ V/V, $R_{id} = 100$ kΩ, and $r_o = 1$ kΩ. Use the feedback analysis.

4-1 (5 分) Identify the feedback topology to be used. (A) Shunt-Series, (B) Series-Series, (C) Shunt-Shunt, (D) Series-Shunt.

4-2 (5 分) Find the voltage gain (V_o/V_s). (A) –96 V/V, (B) –192 V/V, (C) –48 V/V, (D) –108 V/V, (E) -288 V/V.

4-3 (5 分) Find the input resistance R_{in}. (A) 15 Ω, (B) 29.9 Ω, (C) 60 Ω, (D) 1.23 kΩ, (E) 108 kΩ.

4-4 (5 分) Find the output resistance R_{out}. (A) 29.5 Ω, (B) 60 Ω, (C)120 Ω, (D) 1.23 kΩ, (E) 160 kΩ.

5. (20 分)

In a particular CMOS implementation of the shown monostable circuit in Fig. 5, G_1 is a NOR gate and G_2 a simple inverter, both of which use all minimum-sized devices for which (W/L) = 2. For this process, $|V_t| = 1$ V, $\mu_n C_{ox} = 2\mu_p C_{ox} = 20$ μA/V^2, and $V_{DD} = 5$ V. The function of R is implemented using a simple current mirror employing two minimum-sized p-channel devices and a grounded-source diode-connected minimum-width n-channel device of 10 times the minimum length.

5-1 (4 分) Draw the circuit diagram of the simple current mirror employed.

5-2 (4 分) Find V_{OL} of G_1.

5-3 (4 分) Find V_{th} of G_2.

5-4 (8 分) Find the value of C for a 10 μs output pulse, accounting for the non-zero value of V_{OL} of G_1 and the actual value of V_{th} of G_2.

6. (16 分)

Sketch and label the transfer characteristic of the shown circuit in Fig. 6 for $R_1 = 1$ kΩ, $R_2 = 100$ kΩ, $R_3 = 100$ kΩ, with $r_Z = r_D \approx 0$, but $V_Z = 6.8$ V, $V_D = 0.7$ V.

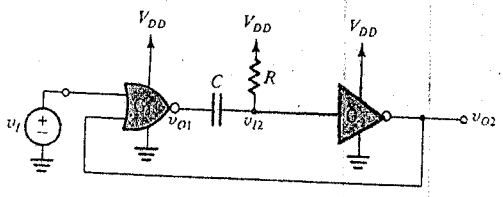

Fig. 5 Monostable circuit for Problem 5.

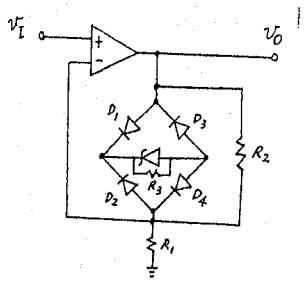

Fig. 6 Circuit for Problem 6