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1. Consider the circuits (a), (b), (c) and (d) shown in Fig.1, assume that every transistor is biased in the forward-active mode and has the same $\beta_F = 100$, $V_{BE(on)} = 0.7$ V, and $V_A = \infty$. If the current sources I_1, I_2, I_3, and I_4 are adjusted such that each Q_1 transistor has the same dc collector current and hence, the same small-signal parameters.

1-1. (8 points) Consider the input resistance R_i, (A) $R_{ia} > R_{ib} > R_{ic} = R_{id}$ (B) $R_{id} > R_{ic} > R_{ib} > R_{ia}$ (C) $R_{id} > R_{ic} = R_{ia} > R_{ib}$ (D) $R_{ib} > R_{ia} = R_{ic} > R_{id}$.

1-2. (8 points) Consider the voltage gain $A_v = |V_{out}/V_{in}|$, (A) $A_{va} > A_{vb} > A_{vc} > A_{vd}$ (B) $A_{vd} > A_{vb} > A_{va} > A_{vc}$ (C) $A_{vd} > A_{vb} > A_{va} = A_{vc}$ (D) $A_{vd} > A_{vc} = A_{va} > A_{vb}$.

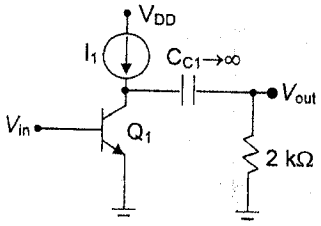

Fig. 1(a)

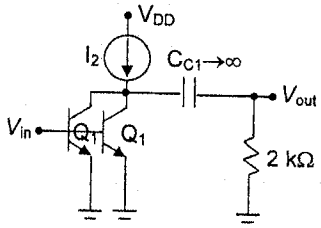

Fig. 1(b)

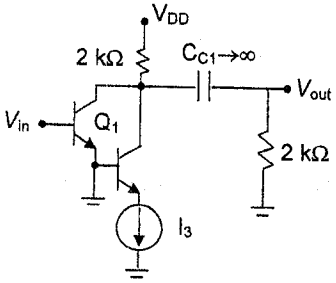

Fig. 1(c)

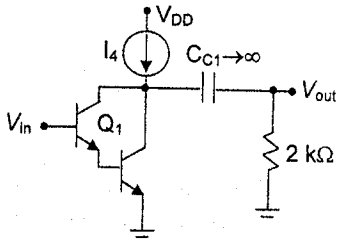

Fig. 1(d)

2. Analyze the high frequency response of the CMOS amplifier as shown in Fig. 2. The dc bias current is 100 μA. For Q_1, $\mu_n C_{ox}$=90 μA/V^2, V_A=12.8V, W/L=100 μm/1.6 μm, and C_{gs}=0.2 pF, C_{gd}=0.015 pF, and C_{db}=20 fF. For Q_2 and Q_3, $\mu_p C_{ox}$=30 μA/V^2, C_{gd}=0.015 pF, C_{db}=36 fF, and $|V_A|$=19.2 V. There is 0.3 pF stray capacitance between the common drain connection and ground. Assume the resistance of the input signal generator is negligibly small, the signal voltage at the gate of Q_2 is zero.

2-1 (3 points) Find g_m for Q_1: (A) 0.106 mA/V, (B) 0.053 mA/V, (C) 1.06 mA/V, (D) 0.212 mA/V, (E) 0.160 mA/V.

2-2 (3 points) Find the output resistance of the amplifier (A) 128 kΩ, (B) 192 kΩ, (C) 320 kΩ, (D) 76.8 kΩ, (E) 160 kΩ.

2-3 (4 points) Find the low frequency voltage gain A_V: (A) –203 V/V, (B) –81.4 V/V, (C) –106 V/V, (D) –135 V/V, (E) -122.1 V/V.

2-4 (6 points) Find the frequency of the zero. (A) 11.25 GHz, (B) 4.75 GHz, (C) 2.38 GHz, (D) 5.625 GHz, (E) 2.81 GHz.

2-5 (6 points) Find the frequency of the pole. (A) 24.1 MHz, (B) 2.41 MHz, (C) 550 KHz (D) 12.02 MHz, (E) 5.37 MHz.

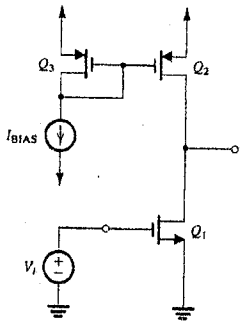

Fig. 2

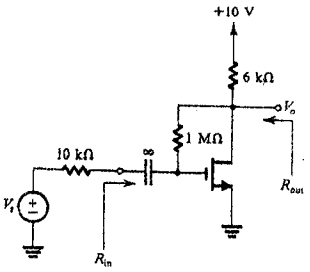

Fig. 3

3. Negative feedback is to be used to modify the characteristics of a particular amplifier for various purposes. Identify the feedback topology to be used if:

3-1 (3 points) Both input resistance and output resistance are to be raised. (A) Shunt-Series, (B) Series-Series, (C) Shunt-Shunt, (D) Series-Shunt.

3-2 (3 points) Input resistance is to be lowered and output resistance raised. (A) Shunt-Series, (B) Series-Series, (C) Shunt-Shunt, (D) Series-Shunt.

A feedback circuit is shown in Fig. 3. Let the parameters of the MOSFET to be V_t=2 V, $\mu_n C_{ox}$ (W/L) =0.5 mA/ V^2.

3-3 (8 points) Find the voltage gain (V_o/V_s). (A) –2.8 V/V, (B) –8.5 V/V, (C) –11.3 V/V, (D) –6.5 V/V, (E) –5.6 V/V.

3-4 (8 points) Find input resistance. (A) 9.34 kΩ, (B) 286 kΩ, (C) 18.68 Ω, (D) 143 kΩ, (E) 160 kΩ.

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4. Fig.4 is the logic diagram of full adder. Please implement this logic circuit by
   (A) (10 points) Static CMOS logic circuit.
   (B) (10 points) Pseudo NMOS logic circuit.

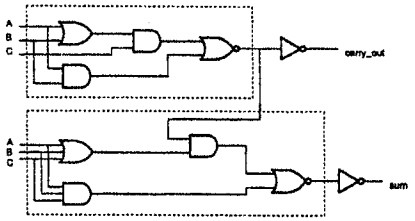

Fig. 4

5. (5 points) Consider a CMOS inverter used for clock with a 20pF capacitive loading; find the dynamic power dissipation when clocked at a 250 MHz rate and the supply voltage is 3 volts.

6. (5 points) Find the D-FF in Fig. 5 is positive or negative clock edge trigger?

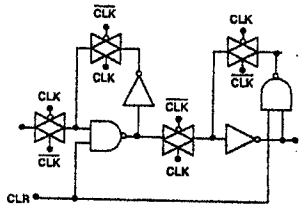

Fig. 5

7. (10 points) Please draw the cross-section diagram of an n- and p-MOSFET in an n-substrate p-well CMOS process.