1. (20%)
   (a) (5%) Describe the principle and application of even-parity code.
   (b) (5%) If $A=41_{10}$, $B=-27_{10}$, express A, B and do A+B by using 8-bit 1's complement number system. The procedure of operation shall be written down.
   (c) (5%) During the addition operation of 1's complement there is an **end-around carry** operation. Explain the principle of the **end-around carry**.
   (d) (5%) Using switching algebra to simplify $(a+b)(\bar{a}+c)(d+b+c)$. The procedure of simplification shall be written down.

2. (20%) Two 2-bit unsigned number ($A=(a_1a_0)_2$, $B=(b_1b_0)_2$) are added together. The sum of these two numbers is sent to a 7-segment display as shown in Fig.1. You are asked to design the logic circuit of this 4-input 7-output *plus-and-display* decoder.
   (a) (5%) Show the complete *truth table* for the *plus-and-display* decoder. "don't care" situation must be considered in your design.
   (b) (10%) Simplify the logic functions of segment y1 and y2 using Karnaugh map. Represent the simplified logic function of y1 in minimum product-of-sum (POS) form. Represent the simplified logic function of y2 in minimum sum-of-product (SOP) form.
   (c) (5%) Use one 4-input/2-output *Programmable Logic Array (PLA)* to realize both y1 and y2 in the same circuit. Use minimum minterms.

3. (15%) A 4-input logic function is as follows.

$$f(a,b,c,d) = \prod M(0,2,4,6,8,10,11,14,15)$$

   (a) (5%) Simplify the logic function of *f* using Karnaugh map. Represent the simplified logic function of *f(a,b,c,d)* in minimum product-of-sum (POS) form.
   (b) (5%) Realize the logic function using only 2-input NOR gates. Show your complete logic circuit. The number of NOR gates should be minimum.
   (c) (5%) Realize the logic function using one *active-high 4-to-1 multiplexer* plus some logic gates. Show your complete logic circuit.

Figure 1. (a) Decimal digits displayed on 7-segment display elements.

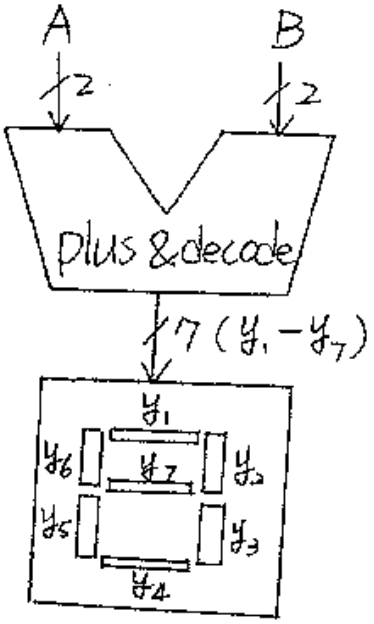

Fig. 1 (b)

注意:背面有試題

參考用

4. (20%)

(a) (5%) In synchronous sequential logic system, there are Mealy Model and Moore Model. Describe the difference of them from logic implementation and timing point of view.

(b) (15%) Using Mealy Model to design a control unit for a simple coin-operated candy machine. Candy costs \$15 and the machine accepts only \$5 and \$10 coins. No more than \$20 can be deposited on a single purchase, and when \$20 is deposited it will returns \$5. Use D flip-flop (Fig. 4) and some logic gates (use as little gates as possible) to design the machine. Your design procedure must be complete, for example, state diagram and so on. You must also use the following variables:

- The input variable: (x1, \$5), (x2, \$10)
- The output variables: (y1, candy), (y2, \$5)
- The state variable assignment (Z1, Z2):

Fig. 4

5. (25%)

Using the block diagram of positive-triggered J-K flip-flop (Fig.5.1) and some logic gates to design

(a) (5%) Synchronous 4 bits serial-in, serial-out shift register. You must draw the complete logic diagram.

(b) (5%) Explain the timing issues such as clock cycle, and the relationship of delay time, set up and hold time of J-K flip-flop in design (a), such that it can function well.

(c) (5%) Asynchronous 4 bits binary counter. You must draw the complete logic diagram.

(d) (5%) Compare the advantages and disadvantages of synchronous and asynchronous counter from logic complexity and timing point of view.

(e) (5%) Using the block diagram of 4 bits binary counter with asynchronous reset (Fig.5.2) and some logic gates to design a modulo-12 counter.

參考用

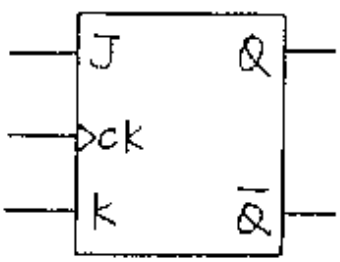

Fig. 5.1

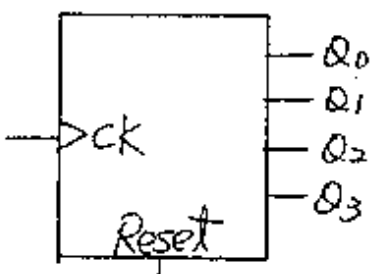

Fig. 5.2