1. (15%) The three MIPS instruction formats are shown below:

Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, imm. format
J-format	op	target address					Jump instruction format

Consider the following while loop in MIPS assembler code:

```
Loop: sll  $t1, $t2, 2      # Temp reg $t1 = t*j
      add  $t1, $t1, $s6    # $t1=address of save[i]
      lw   $t0, 0($t1)      # Temp reg $t0 = save[i]
      bne  $t0, $s5, Exit   # go to Exit if save[i] ≠ k
      addi $s3, $s3, 1      # i = i+1
      j    Loop
Exit: …
```

If we assume the loader places the Loop starting at location 80000 in memory, please determine the values of (a), (b), (c), (d), and (e), respectively, in order to complete the MIPS machine code for the given loop:

80000	0	0	19	9	(a)	0
80004	0	9	22	(b)	0	32
80008	35	9	8	(c)		
80012	5	8	21	(d)		
80016	8	19	19	1		
80020	2	(e)				
80024	…					

2. (10%)

(a) (5%) Suppose that the register `$t1` contains the value of 0x1000 0000$_H$ and the register `$t2` contains the value of 0x10000 0010$_H$. Note that the MIPS architecture utilizes the big-endian addressing. Assume that the data (in hexadecimal) stored in memory at address 0x1000 0000$_H$ is: 0x4433 2211. What value is stored at the register pointed to by the register `$t2`?

```
lbu $t0, 0($t1)
sw  $t0, 0($t2)
```

(b) (5%) Followed by (a), what is the value of the register `$t3` after the following instructions?

```
        slt $t3, $0, $t0
        bne $t3, $0, ELSE
        j   DONE
ELSE:   addi $t3, $t3, 2
Done:
```

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3. (10%) In this problem, we examine how data dependences affect execution in the classical 5-stage pipelined MIPS processor.
   (a) (5%) Assume that there is no delay slot and the branches execute in the ID stage. Assume further that there is full forwarding applied in the datapath. Please indicate hazards and add NOP instructions to eliminate them.

```
add $t1, $s2, $s3
add $t2, $s4, $s5
beq $t1, $t2, Target
```

   (b) (5%) Followed by (a), please indicate hazards and add NOP instructions to eliminate them.

```
lw  $t1, 0($s1)
beq $t1, $s2, Target
```

4. (10%) Consider the following sequence of MIPS instructions being executed on a classical 5-stage pipelined datapath:

```
add r5, r2, r1
lw  r3, 4(r5)
lw  r2, 0(r2)
or  r3, r5, r3
sw  r3, 0(r5)
```

   Assume the following cycle time is required for different implementations:

Without Forwarding	With Full Forwarding
200ps	280ps

   (a) (5%) If there is no forwarding or hazard detection, insert NOP instructions, if necessary, to ensure correct execution. What is the total execution time to execute the code sequence?
   (b) (5%) If the processor has full forwarding, insert NOP instructions, if necessary, to ensure correct execution. What is the total execution time to execute the code sequence?

5. (5%) When a program is running on multiple processors in a multiprocessor system, the execution time on each processor is comprised of computing time and the overhead time required for synchronization and to send data from one processor to another. Assume a program requires t = 100ms of execution time on one processor. When run p processors, each processor requires t/p ms, as well as an additional 40 ms of overhead, irrespective of the number of processors. Please compute for the speedup ratio for p = 8 and p = 16 processors, respectively.

6. [10%] Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5GHz and CPIs of 1, 3, 2, and 2, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

   (a) [3%] The result of the benchmark running on the machine has an instruction count of 2.5E12, and execution time of 800 s, and a reference time of 9000 s. Find the CPI if the clock cycle time is 0.25 ns.

   (b) [3%] Find the increase in CPU time if the number of instructions of the benchmark is increased by 20% and the CPI is increased by 10%.

   (c) [4%] Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D. What is the ratio of CPI for P1/P2?

7. [10%] For the following calculation:
   (a) [3%] Assume 185 and 120 are unsigned 8-bit decimal integers store in sign-magnitude format. Calculate 185+122. As it is overflow, using the saturating arithmetic is needed.

   (b) [3%] Calculate the time necessary to perform a multiply using the approach (31 adders stacked vertically). If an integer is 8 bits wide and an adder takes 5 time unit.

   (c) [4%] What decimal number does the bit pattern 0x0E000000 represent if it is a floating point number? Use the IEEE 754 standard.

8. [10%] For a direct-mapped cache design with 32-bit address [31—0], the following bits of the address are used to access the cache:

Tag field	Index field	Offset field
[31—14]	[13—5]	[4—0]

   (a) [3%] How many entries does the cache have?

   (b) [3%] If 1 bit for the valid field is used, what is the total number of Kibits in a direct-mapped cache?

   (c) [4%] Assume the miss rare of an instruction cache is 4% and the miss rate of the data cache is 3%. The frequency of all loads and stores instruction is 32%. If a processor has a CPI of 2

without any memory stalls and the miss penalty is 100cycles for all misses, how much faster a processor would run with a perfect cache that never missed.

9. [10%] Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses.

   180, 3, 2, 43, 191, 88, 190, 14, 181, 44, 186, 253

   (a) [3%] Assuming the cache is initially empty. For each of these references, given a direct-mapped cache with two-word blocks and a total size of 8 blocks. What is the hit rate?

   (b) [3%] If the miss stall time is 25 cycles and 3 cycles for access time, what is the total cycles for this cache?

   (c) [4%] For a three-way set associative cache (Way-0, Way-1 and Way-2) with two-word blocks and a total size of 24 words. Use LRU replacement. After the last word address "253" is accessed, what is the content of Way-1?

10. [10%] Listed below are key page table parameters. A 4-entry TLB (translation-lookaside buffer) is used.

Virtual address size	Page size	Page table entry size
32 bits	16 KiB	4 bytes

   (a) [3%] Which is the following statement correct?

   A. A larger page size reduces the TLB miss rate.

   B. A larger page size can lead to higher fragmentation and lower utilization of the physical memory.

   C. Fully associative TLB has a lower miss rate.

   D. On page fault, the page must be fetched from disk and write-through is strategy preferred.

   (b) [3%] For a single-level page table, how much physical memory is needed for storing the page table?

   (c) [4%] For a two-level page table approach with 256 entries. Assume each entry of the main page table is 6 bytes. Calculate the minimum amount of memory required for the second-level tables.

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