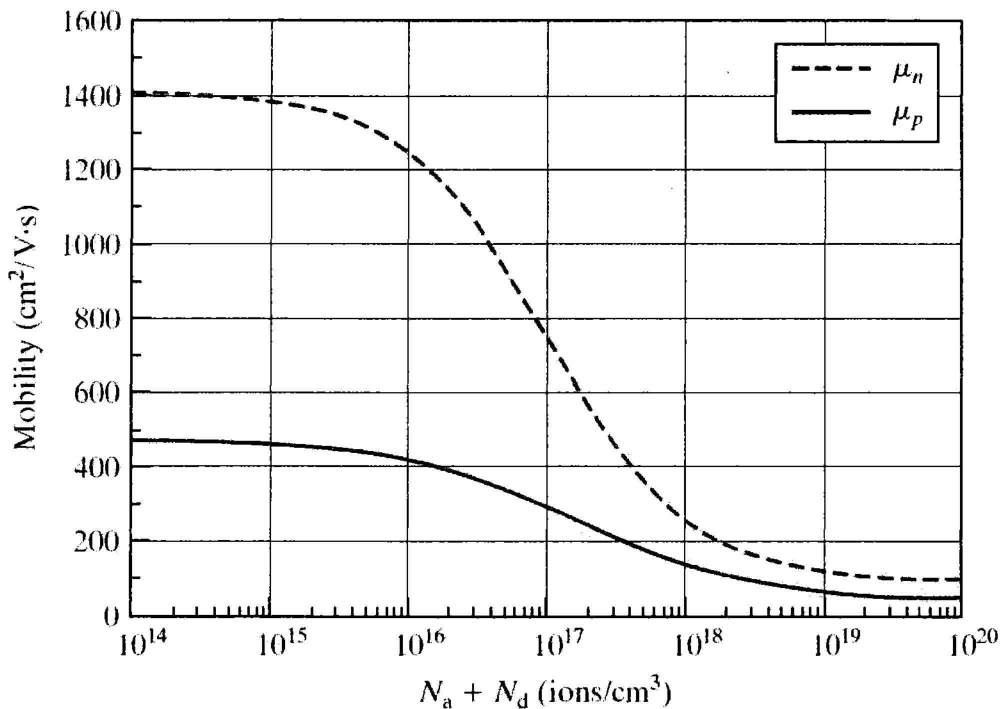
類組：電機類　科目：固態電子元件(300G)　　共 2 頁 第 1 頁

Semiconductor Physics

1. For an N-type silicon sample at room temperature, when an electric field with a strength of 1000 V/cm is applied to the sample, the hole velocity is measured and found to be 2×10^5 cm/sec. At room temperature, use $2.3kT/q = 60$ mV and the intrinsic carrier concentration $n_i = 1 \times 10^{10}$ cm^{-3}.
   (a) Estimate the thermal equilibrium electron and hole concentrations, indicating which is the minority carrier. (5%)
   (b) Find the position of Fermi level E_f with respect to the intrinsic Fermi level E_i, (i.e. $E_f - E_i$). (5%)
   (c) The sample is used to make an integrated circuit resistor. The width and height of the sample are 10 μm and 1 μm, respectively, and the length of the sample is 20 μm. Calculate the resistance of the sample. (5%)

2. For the following 3 N-type silicon samples, find the position of Fermi level E_f with respect to the intrinsic Fermi level E_i at room temperature (i.e. $E_f - E_i$) assuming full ionization for all 3 cases. Check whether the above assumption of full ionization of each case is correct with the calculated Fermi level. Assume the donor level is 0.05 eV below E_c and the energy bandgap $E_g = 1.1$ eV. At room temperature, use $2.3kT/q = 60$ mV and the intrinsic carrier concentration $n_i = 1 \times 10^{10}$ cm^{-3}.
   (a) $N_d = 1 \times 10^{16}$ cm^{-3}. (5%)
   (b) $N_d = 1 \times 10^{18}$ cm^{-3}. (5%)
   (c) $N_d = 1 \times 10^{20}$ cm^{-3}. (5%)



Diodes and BJT

3. Please qualitatively plot the steady-state depletion region widths and the minority carrier concentration profiles in a pn junction under forward bias, zero bias, and reverse bias. Assume that the p-type doping concentration is larger than that of n-type. (15%)
4. The common-base current gain α of an NPN BJT can be expressed as $\alpha = \gamma\alpha_T\delta$ where α is the emitter injection efficiency factor, α_T is the base transport factor, and δ is the recombination factor. To have an α as large (close to 1) as possible, each of these factors must be close to 1 as well. For these three factors, respectively, what about device design and/or operation bias must be done to make them large? (15%) If V_{CE} is increased, will α increase or decrease? Why? (5%)

注意:背面有試題

MOS capacitor and MOSFET

5. Assumed that there is an $Al/SiO_2/p-Si$ metal-oxide-semiconductor (MOS) capacitor. Denote the permittivity of SiO_2 (Si) as ε_{ox} (ε_{Si}) and it is given that the thickness of SiO_2 is t_{ox}, the *p-Si* is uniformly doped to N_A, and the MOS capacitor can be regarded as one-dimensional.

(a) Given that the work function of the *Al* is slightly larger than χ_{Si}, the electron affinity of *Si*, and assumed that the oxide is perfect (completely insulating, no fixed charge/interface states within the oxide and at the interface), please plot the band diagrams of the MOS capacitor when the MOS capacitor is biased at equilibrium and threshold, respectively. You have to include E_{vac} (vacuum level), E_c (conduction band edge), E_i (intrinsic level), E_v (valence band edge) and E_F (Fermi level) in you plots. Please also indicate on you plot the condition that the MOS structure reaches threshold. (10%)

(b) Denote the work function of *Al* as Φ_M. If there is now fixed charges density (per unit area) (Q_F) at the SiO_2/Si interface, write down, without derivation, the threshold voltage (V_{th}) for the MOS capacitor. Note that you have to express the work function of *Si* in term of χ_{Si} and N_A. (6%)

(c) Repeat (b), i.e., write down V_{th}, for an $Al/SiO_2/n-Si$ structure, albeit with N_A replaced by N_D. Denote again the metal work function as Φ_M and express the work function of *Si* in term of χ_{Si} and N_D. (6%)

(d) Explain the difference between enhancement type and depletion type, for both n-channel MOSFET and p-channel MOSFET, in term of threshold voltage. If the $Al/SiO_2/p-Si$ MOS structure in (a) is part of an MOSFET, is this MOSFET enhancement type or depletion type? Repeat for the $Al/SiO_2/n-Si$ MOS structure in (c). (3%, 2%, 2%)

(e) Please explain what CMOS logics are and their advantages over p-MOS/n-MOS technology for VLSIs of high integration level. (6%)