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※請在答案卷內作答

考生請注意

- 本試卷共有 20 題試題。 每題 5 分。
- 你的答案必須如下圖所示由上而下依序寫在答案卷的做答區。
- 只要填寫考題所要求的答案,請勿附加計算過程。

從此處開始寫起
1. (a), (b).
2. (c), (d).
3. 15
4. (1) 1,(2) 0
5. Z = B+AC'



注背面有試題

台灣聯合大學系統 106 學年度碩士班招生考試試題

類組:電機類 科目:數位邏輯(300H)

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※請在答案卷內作答

Question 1 [5pt]. Convert 63.2₇ to a number with base 16.

Question 2 [5pt]. Which of the following equations are valid? (Multiple choices)

- (a) A'B'C+B'CD' + EF' = (B' + E)(B' + F')(C+E)(C+F')(A' + D' + E)(A' + D' + F')
- (b) $WXY' + (W' \equiv X) + (Y \oplus W) = (X + Y) \oplus W$
- (c) [(A' + B')' + (A'B'C)' + C'D]' = A'B'C
- (d) H'I' + JK = (H' + I')(K' + J)(H' + K)(I' + K)

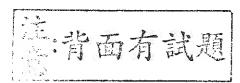
Question 3 [5pt]. Which of the following statements is always true? (Multiple choices)

- (a) If AD' + BD' = CD', then AE + BE = CE.
- (b) If $A \equiv B$ is always **true**, then A(X' + Y + Z') = B(X' + Y + Z') is always valid.
- (c) If $A \oplus B$ is always **true**, and AX = BY is always valid, then XY must be **false**.
- (d) If A + C = B + C, then AZ = BZ.

Question 4 [5pt]. A combinational circuit has three binary inputs (A,B,C) and two binary outputs (X,Y). XY_2 represents a binary number whose value equals the number of 1's at the input. For example, if ABC=011,then XY=10. Choose the correct minterms to form the m-notation of X, where the order of literals for m-notation is ABC. (Multiple choices)

(a) m_0 (b) m_1 (c) m_2 (d) m_3 (e) m_4 (f) m_5 (g) m_6 (h) m_7





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Question 5 [5pt]. The Karnaugh map below shows the function F with four inputs (A, B, C, D), where A is the most significant bit and D is the least significant bit.

AE	3	_		
CD	00	01	11	10
00	х	1	Х	0
01	0	Х	0	Х
11	Х	1	X	1
10	0	Х	1	Х
10	0	х	1	Х

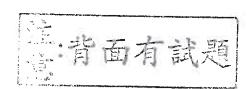


Which of the following statements is true? (Multiple choices)

- (a) If minterm $m_{13} = 1$, then F = 0.
- (b) If F = 0, then maxterms $M_4 = M_7 = M_{11} = M_{14} = 1$.
- (c) If minterms $m_1 = m_2 = m_8 = m_{13} = 0$, then F = 1.
- (d) A'C'D', BC'D', A'B, CD, BC, AC are prime implicants of F.
- (e) F has more than six prime implicants.
- (f) F has no essential prime implicant.

Question 6 [5pt]. Given $F(A, B, C, D) = \prod M(0, 1, 2, 8, 14) \cdot \prod D(3, 5, 7, 9, 10, 15)$. Which of the following statements is true? (Multiple choices)

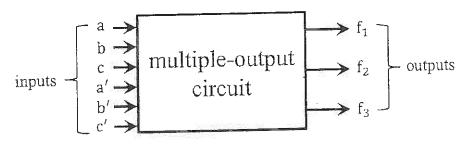
- (a) The minimum sum of product (SoP) for F is unique.
- (b) The minimum sum of product (SoP) for F is A'B + BC' + CD.
- (c) The minimum product of sum (PoS) for F is $(B + D) \cdot (A' + C' + D) \cdot (A + B)$.
- (d) The minimum sum of product (SoP) for F is A'B + BC' + AD.
- (e) The minimum product of sum (PoS) for F is $(B + D) \cdot (A' + C' + D) \cdot (B + C)$.
- (f) Boolean expressions respectively shown in (b) and (c) are equivalent.
- (g) Boolean expressions respectively shown in (b) and (e) are equivalent.
- (h) F has more than three minimum product of sum (PoS) solutions.



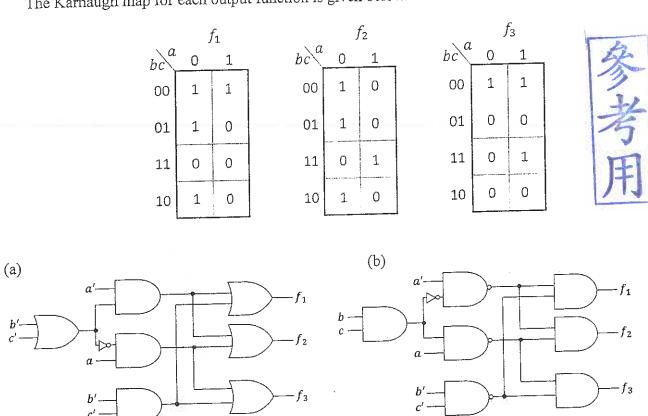
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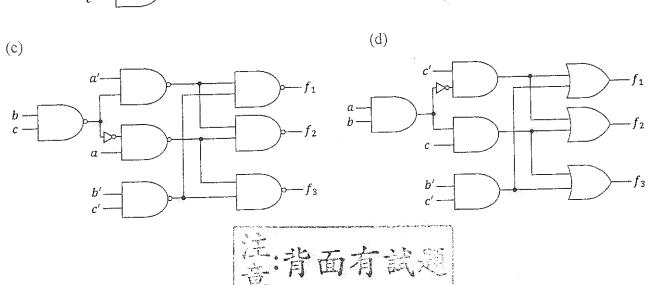
※請在答案卷內作答

Question 7 [5pt]. Choose the circuits which can realize the multiple-output circuit shown in the following figure. (Multiple choices)



The Karnaugh map for each output function is given below.

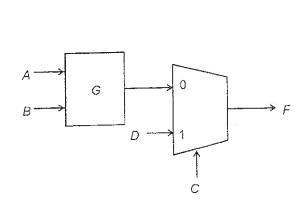




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※請在答案卷內作答

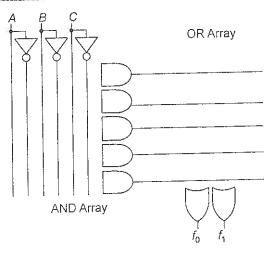
Question 8 [5pt]. Suppose a Boolean function F is implemented by the following circuit with a multiplexor and some unknown function G. In addition, F is partially known shown in the following Karnaugh map. What is the possible function of F in terms of minimum sum of products?



CD AE	3 00	01	11	10
00	?	?	1	?
01	1	?	?	0
11	?	?	?	? :
10	?	?	?	?

Question 9 [5pt]. What is the corresponding function of G in Question 8?

Question 10 [5pt]. Implement $f_1(A, B, C) = \sum m(3, 7)$ and $f_2(A, B, C) = \sum m(1, 2, 5)$ using a PLA. Please complete the design with the minimum form.



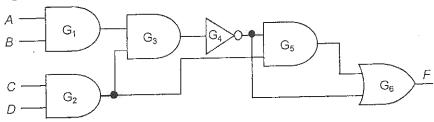




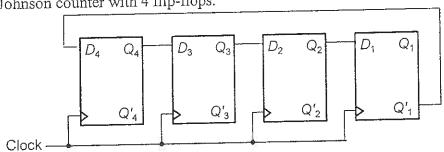
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※請在答案卷內作答

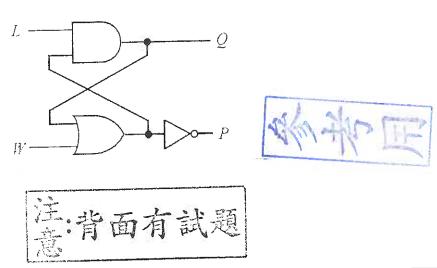
Question 11 [5pt]. Dr. Hunt is debugging a faulty circuit as shown below. According to the specification, with applying the input vector (A, B, C, D) = (0, 0, 1, 1), the output value at F should be 0. However, the actual simulation result is 1. Hunt knows errors come from using wrong gate types. Assume only the following gate types could be misused: AND \leftrightarrow NAND, OR \leftrightarrow NOR, Inverter \leftrightarrow Buffer (one buffer equals two cascaded inverters), and only one error exists in this circuit. Please indicate all possible erroneous gates. (Please write down the gate instance names.)



Question 12 [5pt]. How many states does a Johnson counter with N flip-flops have? The figure below shows a Johnson counter with 4 flip-flops.



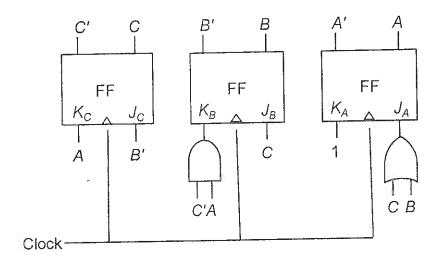
Question 13 [5pt]. A latch design is given below. To guarantee Q will always equal P', what values cannot be placed on L and W?



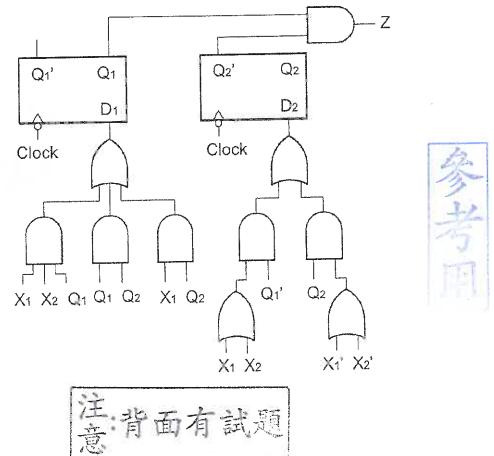
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※請在答案卷內作答

Question 14 [5pt]. Professor Pond received the following circuit diagram of a secret counter implemented by J-K flip-flops. Given that the initial state of CBA is 000, please derive the entire counting sequence of this counter. (000 -> ??? -> ... -> 000)



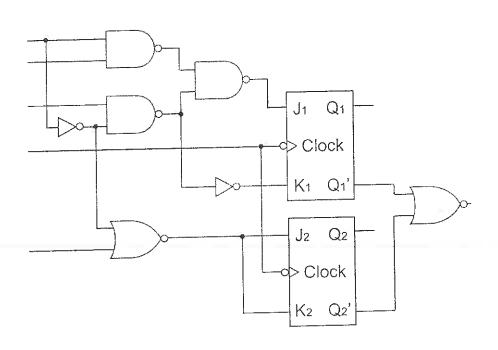
Question 15 [5pt]. For a Moore machine as illustrated in the figure below, if $Q_1Q_2=11$, please identify the values of X_1X_2 to make Z=1 in the next state.



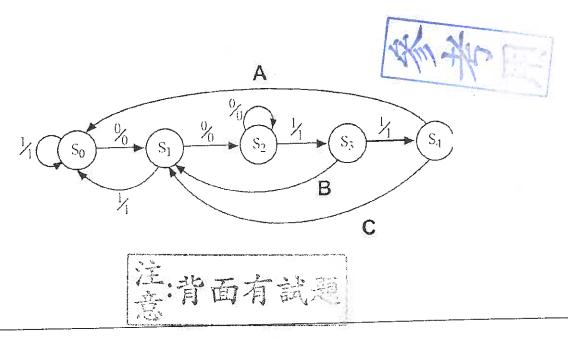
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※請在答案卷內作答

Question 16 [5pt]. The figure below shows a Moore machine. The state variables Q_1 and Q_2 can specify four states. Please identify the state (Q_1Q_2) that will loop to itself (a state that is not connected to other states).



Question 17 [5pt]. The state graph of a Mealy sequential circuit is shown in the figure below. The circuit transmits its input, except that it should prevent the sequence 00100 from occurring. Z should be the same as X, except that if the input sequence 00110 occurs, Z should be 1 rather than 0 when the last 0 is received. So the sequence X=00110 is replaced with Z=00111. Please specify the correct input and output for the three missing transitions (A, B, and C).



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※請在答案卷內作答

Question 18 [5pt]. A Mealy machine has one input X and two outputs (Z_1 and Z_2). The circuit produces an output of $Z_1=1$ whenever the sequence 011 is completed, and an output of $Z_2=1$ whenever the sequence 0111 is completed. The figure below shows the state table. Which state (S_0 to S_3) specifies the state when the machine receives the sequence 011?

State	Next State $X = 0$ $X = 1$		•	$Z_{\frac{2}{X}} = 1$
S_0	S_1	S_0	00	00
S_1	S_{i}	S_{2}	00	00
S	S_1	S_3	00	10
S_3	S_1	S_{0}	00	01

Question 19 [5pt]. A Mealy machine has one input and one output that will produce an output of 1 for every second 0 it receives and for every second 1 it receives.

For example:

The circuit is implemented using two J-K flip-flops. Which of the following logic expressions can meet the specification of the Mealy machine defined above?

- (a) $J_a=X'$, $K_a=1$, $J_b=X$, $K_b=1$
- (b) $J_a=0$, $K_a=1$, $J_b=1$, $K_b=X$
- (c) $J_a=X$, $K_a=X$, $J_b=0$, $K_b=1$
- (d) $J_a=1$, $K_a=X$ ' , $J_b=X$ ' , $K_b=X$
- (e) $J_a=X', K_a=X', J_b=1, K_b=1$
- (f) $J_a=X'$, $K_a=0$, $J_b=X'$, $K_b=1$



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Question 20 [5pt].

Which of the following choices contain tables that are equivalent?

(a)

	XY = 00	01	11	10	Z
a	a	С	е	d	0
b	d	е	е	a	0
C	е	a	f	b	1
d	b	C	C	b	0
е	С	d	f	a	1
f	f	b	а	d	1

	XY = 00	01	11	10_	Z
a	b	i	С	g	0
b	b	C	f	g	0
C	h	d	d	f	1
d	h	C	е	g	1
e	b	C	i	g	0
f	f	į	Ī	k	0
g	j	k	g	h	0
ĥ	e	f	C	g	0
i	j	i	i	d	0
j	Ь	f	C	g	0
k	a	C	е	g	1

(b)

	X = 0	1	
S_0	S ₃	S ₁	0
S ₁	5 ₀	S ₁	0
S_2	So	S_2	1
S_3	S_0	S_3	1

	X = 0	1	
A	Ε	Α	1
В	F	В	1
C	Ε	D	0
D	Ε	C	0
Ε	В	D	0
F	В	C	0

(c)

Present State	<i>X</i> = 0	1	X = 0	1
a	h	С	1	0
b	c	d	0	1
Ċ	h	b	0	0
d	f f	h	0	0
e	С	f	0	1
f	f	g	0	0
0	a	C	1	0
h	a	С	1	0

Present State	<i>X</i> = 0	<i>X</i> = 1	<i>X</i> = 0	<i>X</i> = 1
a	е	g	0	1
Ь	d	f	0	1
С	e	C	1	0
d	Ь	f	0	1
e	q	f	0	1
f	b	d	1	0
g 	е	C	1	0

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