類組：電機類　科目：數位邏輯(300H)　※請在答案卷內作答

考生請注意:

- 本試卷共有 20 題試題。 每題 5 分。
- 你的答案必須如下圖所示由上而下依序寫在答案卷的做答區。
- 只要填寫考題所要求的答案，**請勿附加計算過程**。

從此處開始寫起
1. (a), (b).
2. (c), (d).
3. 15
4. (1) 1 ,(2) 0
5. Z = B+AC'
、、、

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Question 1 [5pt]. Calculate the binary equivalent of $(9/7)_{10}$ out to 8 places. Then convert the result to hexadecimal.

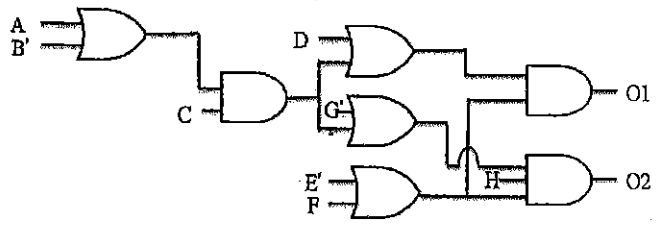
Question 2 [5pt]. Perform subtraction on the following unsigned binary numbers using the 2'-complement of the subtrahend.
(a) 110100 – 10101
(b) 101010 – 101101

Question 3 [5pt]. Simplify the complement of the Boolean function F= (x+ y)(x'+ y'+z')(x+ y'z) in sum of minterms, and draw its logic diagram.

Question 4 [5pt]. Simplify the Boolean function F(*w, x, y, z*) =Σ (1, 4, 5, 6, 7, 12, 13, 14, 15) in product of sums using four-variable Karnaugh maps.

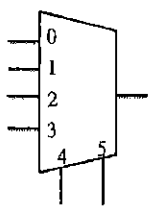
Question 5 [5pt]. Simplify the following Boolean expressions to a minimum number of literals:
(a) (x+y) (x'+y') (x+y')
(b) xyz + x'y + y'z + xyz'

Question 6 [5pt]. Convert this circuit to an implementation with minimum number of 2-input NAND gates and NOT gates. How many NOT gates are needed in this implementation? Note that the implementation should use the same inputs and outputs.



Question 7 [5pt]. How many NAND gates are needed to implement a minimum two-level, multiple-output NAND-NAND circuit that realizes the following two functions?
$f_1 = \Sigma m(0, 2, 4, 6, 7, 10, 14)$ and $f_2 = \Sigma m(0, 1, 4, 5, 7, 10, 14)$

Question 8 [5pt]. Use one 4-to-1 multiplexer to realize the function f(a,b,c,d) = ∑m(1,5,6,8,9,12)+ ∑d(13,14). Please specify the signal to each input of the 4-to-1 multiplexer, following the order (0, 1, 2, 3, 4, 5).



Question 9 [5pt]. The function F = CD'E + CDE + A'D'E + A'B'DE' + BCD is implemented in an FPGA with F = B'C' (F_0) +B'C(F_1) + BC'(F_3) + BC(F_4). Please write down the minterm expressions of the three-variable functions F_0(A,D,E), F_1(A,D,E), F_2(A,D,E), and F_4(A,D,E).

Question 10 [5pt]. Implement the function F=CD'E + CDE + A'D'E + A'B'DE' + BCD using 3-variable lookup tables. Please fill the missing entries in the truth table.

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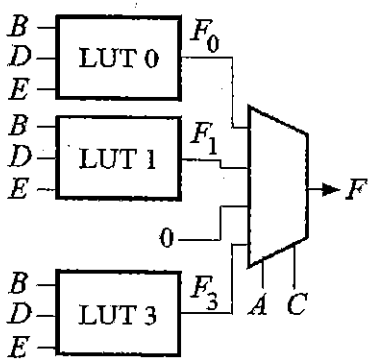


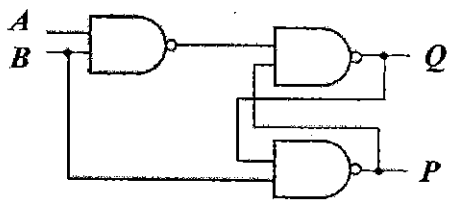
BDE	F_0 F_1 F_3
000	0 0 0
001	1 1 1
010	
011	
100	0 0 0
101	
110	
111	

Question 11 [5pt]. A new-type *AB* latch operates as follows: If $A = 0$ and $B = 0$, the latch state is $Q = 0$; if either $A = 1$ or $B = 1$ (but not both), the latch output does not change; and when both $A = 1$ and $B = 1$, the latch state is $Q = 1$. Derive the characteristic equation for this *AB* latch.

$Q^+ =$ ____ + ____ + ____

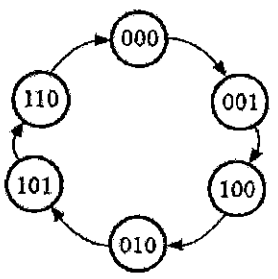
Question 12 [5pt]. For the latch circuit below, derive the next-state equation for this circuit using Q as the state variable and P as an output.

$Q^+ =$ ____ + ____



Question 13 [5pt]. The first D flip-flop C in the state graph below can be used to generate the sequence 0, 0, 1, 0, 1, 1 and repeat. Derive the characteristic equation for the first flip-flop. Do not duplicate states and use the fewest number of gates.

$C^+ =$ ____ + ____



Question 14 [5pt]. A 3-bit counter that counts in the sequence: 001, 011, 010, 110, 111, 101, 100, (repeat) 001, … is realized by D flip-flops. What is the next state if the counter is started in state 000?

Question 15 [5pt]. For the circuit below, list the output values produced by an input sequence $X = 10111$. (Assume that initially $Q_1 = Q_2 = 0$ and that X changes midway between the rising and falling clock edges.)

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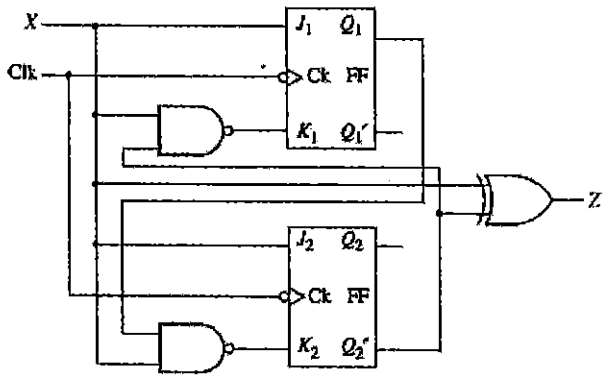
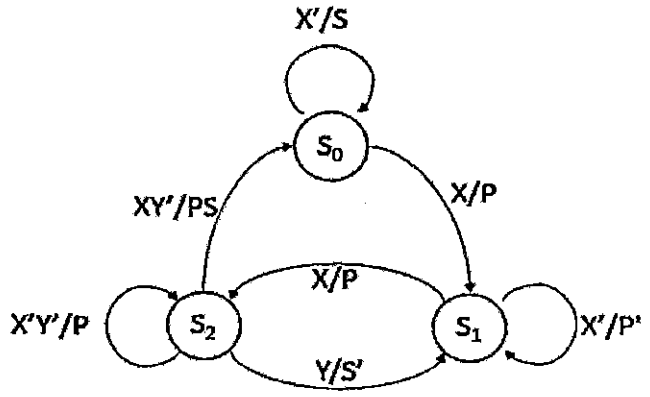


Question 16 [5pt]. Following shows the state graph of the targeted circuit, which contains two inputs (denoted as X and Y), two outputs (denoted as P and S) and three D flip-flops (denoted as Q_2, Q_1, and Q_0). A one-hot assignment is used here to implement the circuit, where $S_0(Q_2Q_1Q_0) = 001$, $S_1(Q_2Q_1Q_0) = 010$, and $S_2(Q_2Q_1Q_0) = 100$. Please write down the next-state equation of Q_1 (denoted as Q_1^+).



Question 17 [5pt]. Reduce the following state table to the minimum number of states. Please list all the equivalent states in the original state table. (For example, i=j=k, l=m.)

Present State	Next State		Present Output
	X=0	X=1	
a	d	c	0
b	f	h	0
c	e	d	1
d	a	e	0
e	c	a	1
f	f	b	1
g	b	h	0
h	c	g	1

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Question 18 [5pt]. The targeted sequential circuit has one input X and one output Z. The values of Z at the first three clock cycles are all 1s. The later value of output Z is determined by the values of input X at three cycles before (denoted as P), two cycles before (denoted as Q) and one cycle before (denoted as R). If $P + QR = 1$, then the value of output Z is 1. Otherwise, the value of output Z is 0. The following table shows an exemplary input/output sequence of the targeted sequential circuit.

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	0	1	0	1	0	1	1	0	0	1	1	1	0	0	1
Z	1	1	1	0	1	0	1	1	1	1	0	1	1	1	1

The corresponding state table of the targeted sequential circuit is given in the following. Please list the missing slots (a), (d), and (f) in the state transition table, respectively.

Present State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
S_0(Reset)	S_1	S_0	1	1
S_1	S_6	S_2	1	1
S_2	S_4	S_0	1	1
S_3	(a)	(b)	0	0
S_4	(c)	(d)	0	0
S_5	S_4	S_0	0	0
S_6	S_3	S_5	(e)	(f)

Question 19 [5pt]. Following first shows the state transition table of a circuit, which converts a serial excess-3 code at input X to the corresponding BCD code at output Z with the last significant bit first. We use a PLA and three D flip-flops to implement the circuit. The PLA table is shown below the transition table. Please list the missing slots (a), (b), (c), and (d) in the PLA table.

Transition table				
Present states $Q_1Q_2Q_3$	Next states $Q_1^+Q_2^+Q_3^+$		Output Z	
	X = 0	X = 1	X = 0	X = 1
000(Reset)	111	101	1	0
001	100	110	1	0
011	110	110	0	1
010	xxx	xxx	x	x
100	xxx	000	x	0
101	001	011	1	0
111	001	001	0	1
110	000	000	0	1

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PLA table		
Product term	Inputs	Outputs
	$XQ_1Q_2Q_3$	$ZQ_1^+Q_2^+Q_3^+$
$X'Q_1'Q_3'$	00−0	0010
$X'Q_2'$	0−0−	1000
$Q_1'Q_3'$	−0−0	0001
Q_1'	−0−−	(a)
$Q_1'Q_2$	−01−	0010
Q_1Q_3	−1−1	(b)
$XQ_2'Q_3$	1−01	(c)
XQ_2	1−1−	(d)
	AND plane	OR plane

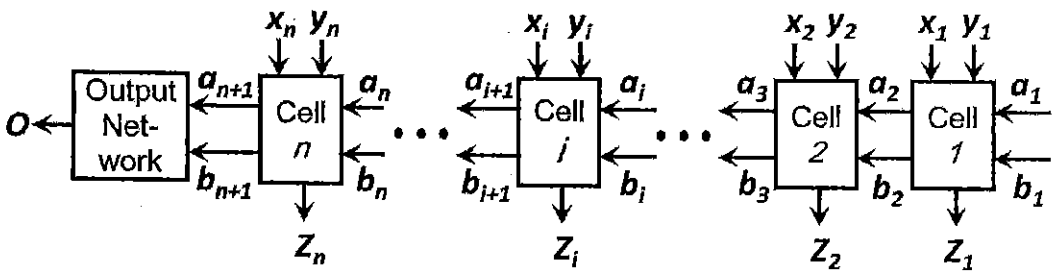
Question 20 [5pt]. The specification of an iterative circuit called the "subtractor" is described as follows.

I. The inputs include two n-bit unsigned binary values $X = x_n x_{n-1} \dots x_2 x_1$ and $Y = y_n y_{n-1} \dots y_2 y_1$

II. The outputs include a 1 bit value O and an n-bit unsigned binary value $Z_n \dots Z_1$.
If $X \geq Y$, then $O = 0$ and $Z_n \dots Z_1$ represents the result of $X - Y$
If $X < Y$, then $O = 1$ and $Z_n \dots Z_1$ represents the result of $X_{new} - Y_{new}$ where $X_{new} = 1x_n x_{n-1} \dots x_2 x_1$ and $Y_{new} = 0y_n y_{n-1} \dots y_2 y_1$ (both of them are n+1 bit unsigned binary value)

Please choose a circuit which can meet the specification of the iterative circuit from (a) to (f).

(a) A circuit which has the following circuit diagram with $a_1 = 0$, $b_1 = 0$, and $O = a_{n+1}b_{n+1}$



Cell i calculates a_{i+1}, b_{i+1}, and Z_i by the following equations for $i = 1 \sim n$.
$a_{i+1} = x_i'y_i'b_i + x_ib_i' + x_ia_i$ and $b_{i+1} = x_i'a_i + y_ib_i' + x_iy_i'b_i$
$Z_i = y_i' + x_i'y_ia_ib_i' + x_ib_i$

(b) A circuit which has the same circuit diagram as (a) with $a_1 = 1$, $b_1 = 0$, and $O = a_{n+1}b_{n+1} + a_{n+1}'b_{n+1}'$
Cell i calculates a_{i+1}, b_{i+1}, and Z_i by the following equations for $i = 1 \sim n$.
$a_{i+1} = x_ia_ib_i + x_i'y_ia_i'b_i + y_ia_i' + x_iy_i$ and $b_{i+1} = x_i'y_i'b_i + x_i'y_ia_ib_i + x_ib_i$
$Z_i = x_iy_i + x_i'y_ib_i + x_ia_i$

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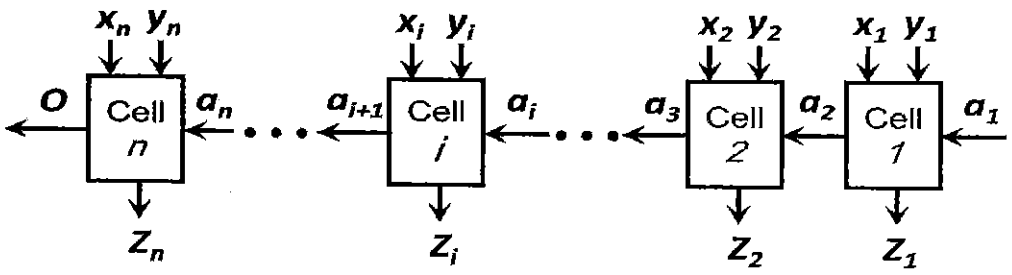
(c) A circuit which has the following circuit diagram with $a_1 = 0$ and $O = a_{n+1}$



Cell i calculates a_{i+1} and Z_i by the following equations for $i = 1 \sim n$.

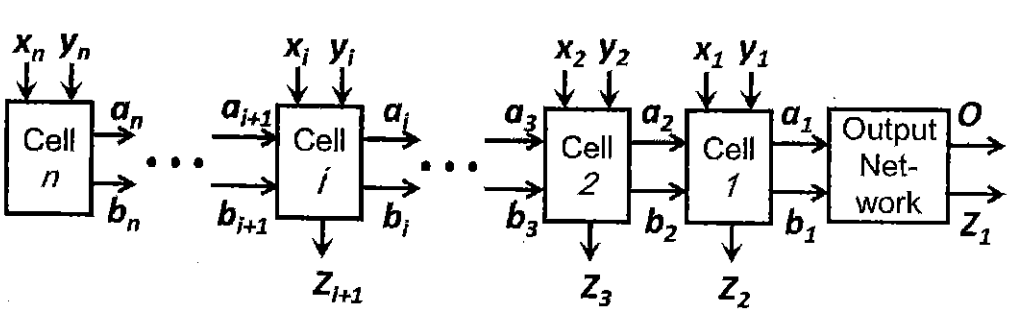
$a_{i+1} = x_i' + x_i a_i + x_i y_i$ and $Z_i = x_i{}' a_i + x_i y_i{}' a_i{}' + y_i a_i{}'$

(d) A circuit which has the same circuit diagram as (c) with $a_1 = 0$ and $O = a_{n+1}$

Cell i calculates a_{i+1} and Z_i by the following equations for $i = 1 \sim n$.

$a_{i+1} = x_i{}' a_i + y_i a_i + x_i{}' y_i$ and $Z_i = x_i y_i a_i + x_i{}' y_i{}' a_i + x_i{}' y_i a_i{}' + x_i y_i{}' a_i{}'$

(e) A circuit which has the following circuit diagram with $Z_1 = a_1 b_1 + a_1{}' b_1{}'$ and $O = a_1{}' b_1{}'$



Cell i calculates a_i, b_i, and Z_{i+1} by the following equations for $i = 1 \sim n-1$.

$a_i = x_i{}' y_i{}' b_{i+1}{}' + x_i y_i a_{i+1} b_{i+1}{}' + x_i{}' y_i a_{i+1} b_{i+1}$

$b_i = x_i{}' y_i + x_i y_i{}' b_{i+1} + x_i y_i a_{i+1}$

$Z_{i+1} = x_i a_{i+1}{}' + y_i a_{i+1}{}' b_{i+1} + x_i y_i{}' a_{i+1}{}' b_{i+1}{}'$

Cell n calculates a_n and b_n by the following equations.

$a_n = x_n y_n{}'$

$b_n = x_n{}' y_n$

(f) A circuit which has the same circuit diagram as (e) with $Z_1 = a_1{}' b_1 + a_1 b_1{}'$ and $O = a_1 b_1{}'$

Cell i calculates a_i, b_i, and Z_{i+1} by the following equations for $i = 1 \sim n-1$.

$a_i = x_i{}' y_i a_{i+1} b_{i+1} + y_i a_{i+1}{}' b_{i+1} + x_i b_{i+1}{}'$

$b_i = y_i' a_{i+1} + x_i{}' a_{i+1}{}' b_{i+1} + x_i a_{i+1} b_{i+1}{}'$

$Z_{i+1} = y_i a_{i+1} b_{i+1}{}' + x_i y_i{}' a_{i+1} b_{i+1}$

Cell n calculates a_n and b_n by the following equations.

$a_n = x_n{}' y_n{}'$

$b_n = x_n y_n$