1. 簡答題：(每題 5 分，共 25 分)
   a. Explain the Booth's Algorithm for integer multiplication.
   b. What is the concept of RISC?
   c. List at least three kinds of pipeline hazards.
   d. What is superscalar processor?
   e. Show the IEEE 754 binary representation of the number -0.75 in single precision (32 bits) and double precision (64 bits).
2. (5%) (a) What is the Amdahl's Law? According to this law, what can parameters *x*, *y*, and *z* be in the following formula:

$$\text{speedup} = \frac{1}{x + (y/z)}$$

   (5%) (b) Given a problem in which at most 20% portion can be parallelized, what is the maximal speedup you can obtain according to the Amdahl's Law?
3. (5%) (a) What is loop unrolling?
   (10%) (b) We assume a RISC processor with pipelining. Given a high-level program:

```
for (i=n; i > 0; i--)
    A[i] = A[i] + 999;
```

   suppose the program is translated into an assembly code as follows:

```
// Initially, register R1 points to A[n].
loop:  LOAD    R2, 0(R1)      //load A[i] to R2
       ADD     R2, R2, #999   //add immediate 999 to R2
       STORE   0(R1), R2      //store the result
       SUB     R1, R1, #1     //decrement R1
       BNEZ    R1, loop       //branch if R1 is not zero
```

   To execute the program in a pipelined manner, suppose one stall must be inserted (i) between LOAD and ADD, (ii) between ADD and STORE, (iii) SUB and BNEZ. Except these, no other stalls are needed. How do you apply the loop unrolling technique to reduce the stalls? (Note: the more efficient you program is, the more credits you may get. Assume that there are 16 general-purpose registers.)

4. (5%) (a) What is branch prediction in CUP design?
   (5%) (b) Design a 1-bit branch predictor (guess taken or untaken based on the behavior of the previous branch).
   (5%) (c) Design a 2-bit branch predictor (guess taken or untaken based on the behavior of the previous two branches).
   (5%) (d) What are the advantages and disadvantages of the 2-bit predictor over the 1-bit predictor. Explain your answer.
5. (10%) A sequential network has one input and one output. If the input sequence is 0101 or 0110, then an output of two successive 1's will occur. The network should reset when the second output 1 occurs. For example:

   ```
   input sequence = 010011101010101101 ...
   output sequence= 000000000011000011 ...
   ```

   Derive a Mealy state table and diagram for this network.
6. (10%) Develop a 4-bit cyclic shift register using 4 S-R flip-flops. The cyclic shift register should be driven by a clock.
7. (10%) A CPU has a cache of size 8 Kbytes. Each block is 32 bytes. The cache data is byte-addressable (i.e., each byte in a block can be specified and addressed). Show the cache design when
   (a) a direct mapped strategy is used
   (b) a 2-way set associative is used