國立中央大學八十六學年度碩士班研究生入學試題卷

1. Design a 3-to-8 decoder from a 2-to-4 decoder and several 2-input AND gates. (10%)

2. Please state two drawbacks if we use the MIPS (or MFLOPS) to evaluate the performance of a machine. (10%)

3. A non-pipelined processor X has a clock rate of 100 MHz and an average CPI (cycles of per instruction) of 4. Processor Y, an improved successor of X, is designed with a five-stage linear instruction pipeline. However, due to latch delay and clock skew effects, the clock rate of Y is only 75 MHz. If a program containing 1000 instructions is executed on both processors, what is the maximum speedup of processor Y compared with that of processor X? (10%)

4. Please give at least two reasons why the performance of a machine will be significantly affected by the compilers. (10%)

5. We can design a processor with single clock cycle or multiple clock cycle implementations. In the single-cycle implementation, the clock cycle must have the same length for every instruction, and the CPI will therefore be 1. On the other hand, the multiple-cycle implementation allows instructions to complete in different numbers of clock cycles. If you are a architect which one of implementations shall be used and why? Note that, the clock cycle time of the multiple-cycle implementation is smaller than the single-cycle implementation. (10%)

6. Pipelining is an implementation technique in which multiple instructions are overlapped in execution. However, conditional branch can delay the next instruction fetch, Please give two methods to solve the branch hazards. (10%)

7. In a pipeline machine, multiple exceptions can occur simultaneously by different instructions. Give a solution to handle the multiple exceptions case. (10%)

8. Please state two important advantages of the memory hierarchy. (10%)

9. A certain memory system has a 32 MB main memory, and a 64 KB cache. Blocks are 16 bytes in size. Assume the physical memory address is 30 bits. Please show the tag size if the cache is (a) associative (b) directed-mapped. (10%)

10. Why does DMA (Direct Memory Access) have priority over the CPU when both request a memory transfer? (10%)