國立中央大學八十五學年度碩士班研究生入學試題卷

所別：資訊工程研究所　不分組　科目：計算機結構　共 1 頁 第 1 頁

1. If a CPU receives multiple requests for exceptions at about the same time, it should service all of them before returning control to the interrupted program. What type of mechanism should it use for holding the interrupt requests: a queue, a stack, or something else? Explain. (10%)

2. Explain why DMA I/O is faster than CPU-controlled I/O. (15%)

3. Consider a virtual memory system with the following properties: 36-bit virtual address, 4 KB pages, and 32-bit physical address. What is the total size of the page table for each process on this machine, assuming that the valid, protection, dirty, and use bits take a total of 4 bits and that all the virtual pages are in use. Assume that disk addresses are not stored in the page table. (15%)

4. Suppose you have a 4 words cache with a block size of 1 word. Consider the following list of references to words being read from memory: 2, 4, 1, 3, 1, 2, 0, 4, 3, 1. Assume the cache initially empty. Assuming the cache is fully-associative using an LRU replacement policy, label each of the references as either a hit (H) or a miss (M) and show the final contents of the cache. (15%)

Address	2	4	1	3	1	2	0	4	3	1
H or M										

Address

Final contents of cache

5. Pipelining is an implementation technique in which multiple instructions are overlapped in execution. Under ideal conditions, the maximum speedup from pipelining equals the number of pipe stages. Identify as many reasons as you can why we can not get the maximum speedup usually. (20%)

6. Please explain the following terms: (25%)

   a. Write-back cache
   b. Microprogramming
   c. Interleaved memory
   d. Temporal locality
   e. SIMD machine