

國立中央大學 108 學年度碩士班考試入學試題

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所別：資工類

科目：作業系統與計算機組織

本科考試禁用計算器

單選題(一題 5 分，答錯倒扣 2 分)，倒扣到該大題 0 分為止。

1. Consider a multi-programmed system with degree of 6, that is, six programs in memory at the same time. Assume that each process spends 40% of its time waiting for I/O. What will be the CPU utilization?
(A) 0.6
(B) 0.986176
(C) 0.953344
(D) 0.995904
(E) None of the above
2. A computer system has the following properties: instruction miss rate = 2%, data miss rate = 4%, the percentage of instructions executing data memory access = 20% and miss penalty = 50 clock cycles. Assume that there is no penalty for a memory hit (CPI=1). Calculate the number of clock cycles, H, required to execute a program with 1111 instructions. What is the value of "Round(H) mod 5"? ("mod" is the modulo operator.)
(A) 0 (B) 1 (C) 2 (D) 3 (E) 4
3. A, B, C and D are four IEEE754 single-precision floating-point values. A is the largest denormalized number. B is the smallest positive normalized number. C=-2.25. D represents positive infinity. Now E= A XOR B XOR C XOR D. The number of "1" in E is "K". What is "K mod 5"?
(A) 0 (B) 1 (C) 2 (D) 3 (E) 4
4. Given a 16-word two-way set associative cache with two-word blocks, for the following word address memory access: 12, 17, 18, 16, 5, 29, 19, 12, 4, 22, 23, 24, 17, 25, 26, 27, assume that LRU is used and the number of hit is "K". What is "K mod 5"?
(A) 0 (B) 1 (C) 2 (D) 3 (E) 4
5. For a pipelined implementation, assume that 1/4 of the load instructions are immediately followed by an instruction that uses the result, half of the branches are miss-predicted with 1 clock cycle delay, and jumps always cause 1 clock cycle of delay. If the instruction mix is 24% loads, 20% stores, 30% ALU instructions, 20% branches, and 6% jumps. The average CPI is "K". What is "Round(K*234) mod 5"?
(A) 0 (B) 1 (C) 2 (D) 3 (E) 4

參考用

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多重選擇(一題 5 分，答錯不倒扣)

6. Which of the following statements are true:
- (A) Superscalar machines main rely on hardware to achieve instruction-level parallelism.
 - (B) Page table is a cache.
 - (C) TLB is a cache.
 - (D) The major advantage of microprogramming control is its speed.
 - (E) The case that "TLB hit but cache miss" is possible.
7. Which of the following statements are true for the single-cycle CPU design and the multi-cycle CPU design?
- (A) The clock rate of the multiple-cycle CPU design is larger than single-cycle CPU design.
 - (B) The CPI of the single-cycle CPU is 1.
 - (C) The throughput of the single-cycle CPU is larger than multiple-cycle CPU.
 - (D) The cycle time of the multi-cycle CPU is determined by the slowest instruction.
 - (E) All the above.
8. Consider the following MIPS instructions.
- ```
add $s0, $t0, $t1
sub $t2, $s0, $t3
```
- Which of the following statements are true?
- (A) There is a Read-After-Write hazard .
  - (B) There is a Write-After-Write hazard.
  - (C) We may use data forwarding to solve the above Read-After-Write hazard.
  - (D) We may insert bubbles to solve the above Write-After-Write hazard.
  - (E) All the above.
9. Which of the following statements are true for branch instructions and branch prediction?
- (A) The jump instruction in MIPS is a conditional branch instruction.
  - (B) A branch target buffer is used by the compiler to make predictions.
  - (C) Branch prediction is more important when pipelines are longer.
  - (D) When branch prediction fails, we need to flush instructions and correct PC.
  - (E) All the above.

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10. Consider a pipelined CPU with the following five stages like MIPS: Instruction Fetch (IF), Instruction Decode (ID), Execution (EXE), Memory Access (MEM), and Register Write Back (WB). Which of the following statements are true?

- (A) Compared with non-pipelined CPU, the speed up can be up to twice the number of stages.
- (B) In order to resolve control hazard, we should move the branch execution from MEM to IF.
- (C) Instruction work at each stage should be imbalanced to improve pipeline performance, because such a design allows some stages do more work.
- (D) Branch hazard is due to a data cache miss.
- (E) None of the above.

11. The MIPS instructions of a program are composed as follows.

|     |      |     |     |     |
|-----|------|-----|-----|-----|
| add | addi | beq | lw  | sw  |
| 30% | 20%  | 25% | 15% | 10% |

Which of the following statements are true?

- (A) The instruction memory is used by 50% of the cycles.
- (B) The data memory is used by 25% of the cycles.
- (C) The input of the sign-extended circuit is used by 70% of the cycles.
- (D) The MemtoReg signal is on for 25% of the cycles.
- (E) None of the above.

12. Some computer systems do not provide a privileged mode of operation in hardware.

An operating system for a machine of this type would need to remain in control (or monitor mode) at all times. This could be accomplished by the following methods:

- (A) Software interpretation of all user programs.
- (B) All programs are written in high-level languages. The compiler would generate the protection checks that the hardware is missing.
- (C) Program executing in cloud server.
- (D) Open sourced user program.
- (E) ROM-based operating system.

13. Consider a preemptive priority scheduling algorithm based on dynamically changing priorities. Larger priority numbers imply higher priority.

When a process is waiting for the CPU (in the ready queue, but not running), its priority changes at a rate A ; when it is running, its priority changes at a rate B. All processes are given a priority of 0 when they enter the ready queue. The parameters A and B can be set to give many different scheduling algorithms.

What is the algorithm that results from  $A < B < 0$ ? Or  $A > B > 0$ ?

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- (A) RR
- (B) FCFS
- (C) SJF
- (D) LIFO
- (E) Random

14. Consider a multiprocessor system and a multithreaded program written using the many-to-many threading model. Let the number of user-level threads in the program be more than the number of processors in the system. What are the lower performance implications of the following scenarios.

- (A) The number of kernel threads allocated to the program is less than the number of processors.
- (B) The number of kernel threads allocated to the program is equal to the number of processors.
- (C) The number of kernel threads allocated to the program is greater than the number of processors but less than the number of userlevel threads.
- (D) The number of kernel threads allocated to the program is equal to two.
- (E) The number of kernel threads allocated to the program is greater than the number of processors and also greater than the number of userlevel threads.

15. In a real computer system, neither the resources available nor the demands of processes for resources are consistent over long periods (months). Resources break or are replaced, new processes come and go, new resources are bought and added to the system. If deadlock is controlled by the banker's algorithm, which of the following changes can be made safely (without introducing the possibility of deadlock), and under what circumstances?

- (A) Increase Available (new resources added)
- (B) Decrease Available (resource permanently removed from system)
- (C) Increase Max for one process (the process needs or wants more resources than allowed).
- (D) Decrease Max for one process (the process decides it does not need that many resources)
- (E) Decrease the number of processes

16. Consider the following page reference string:

7, 2, 3, 1, 2, 5, 3, 4, 6, 7, 7, 1, 0, 5, 4, 6, 2, 3, 0, 1.

Assuming demand paging with three frames, how many page faults would occur for the following replacement algorithms?

- LRU replacement

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- FIFO replacement
- Optimal replacement

Select the correct answers:

- (A) 18 for LRU
- (B) 17 for LRU
- (C) 17 for FIFO
- (D) 13 for LRU
- (E) 13 for optimal replacement

17. Two threads from different processes share:

- (A) Global variables
- (B) Heap
- (C) File descriptors
- (D) Program counter
- (E) None of the above

18. CPU scheduling decisions may take place when a process

- (A) Switches from the running state to the waiting state
- (B) Switches from the waiting state to the ready state
- (C) Switches from the ready state to the running state
- (D) Switches from the running state to the decision state
- (E) None of the above

19. Choose the correct statements from the multiple choices

- (A) A smaller page size leads to smaller page tables.
- (B) A smaller page size leads to more TLB misses.
- (C) The Round robin (RR) scheduling algorithm optimizes CPU throughput.
- (D) The Round robin (RR) scheduling algorithm is preemptive.
- (E) None of the above.

20. Choose the correct statements from the multiple choices regarding networking.

- (A) ARP protocol is used to discover a MAC address, associated with a given IP address.
- (B) DNS translates domain names to IP addresses.
- (C) IPSec can be used in VPNs.
- (D) ICMP messages can be used for diagnose errors in IP operations.
- (E) None of the above.

參考用