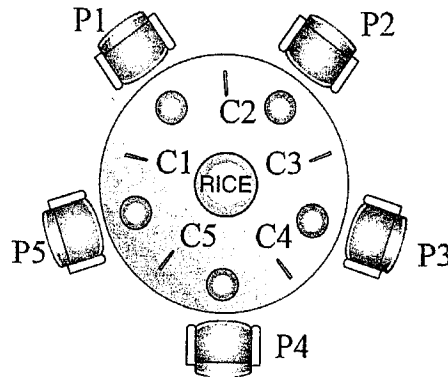


1. (12 points) For the dining philosophers problem, assume it has reached the deadlock state that each philosopher,  $P_i$ , has acquired the chopstick on his right-hand side,  $C_i$ , where  $1 \leq i \leq 5$ . Please draw (a) the resource allocation graph and (b) the wait-for graph for the philosopher deadlock situation.



2. (7 points) The Dynamic Host Configuration Protocol (DHCP) protocol allows a client to dynamically obtain its IP addresses from DHCP server when it joins the network.
- (a) (4 points) There are four phases for the DHCP operations. What phases deliver unicast messages?
- (b) (3 points) During the DHCP operation procedure, how can the client be reached by unicasting before the client obtains its IP address from the DHCP server?
3. (3 points)  
 The sudo command on a Linux system allows a user to:
- (A) suspend the execution of a selected process  
 (B) invoke the execution of a suspended process  
 (C) temporarily assume the identity of the superuser  
 (D) reboot the system  
 (E) none of the above

注意：背面有試題

4. (3 points)  
When a process is created using the classical fork() system call, which of the following are NOT inherited by the child process from the parent process?  
(A) process address space  
(B) process ID  
(C) user ID  
(D) process group ID  
(E) none of the above
5. (5 points) Which of the following components of program state are shared across threads in a multithreaded process? (A). Register values (B).Heap memory (C).Global variables (D).Stack memory
6. (5 points) Explain why implementing synchronization primitives by disabling interrupts is not appropriate in a single-processor system if the synchronization primitives are to be used in a user-level program.
7. (a)(5 points) What is the relationship between a guest operating system and a host operating system in system like VMware?  
(b)(5 points) What factors need to be considered in choosing the host operating system?
8. (5 points) What are the advantages of the variant of linked allocation that uses a FAT (File Allocation Table) to chain together the block of a file?
9. (18 points)  
(a) (3 pts.) Using separated instruction cache and data cache instead of a unified cache could mainly reduce which kind of hazard?  
(A) Control hazard (B) Structural hazard (C) Data hazard (D) None of above  
(b) (3 points) The motivations of dynamic scheduling do NOT include:  
(A) Hide memory latency (B) Avoid stalls that compilers could not schedule  
(C) Prevent out-of-order completion (D) Speculatively execute instructions while waiting for hazards to be resolved

注意：背面有試題

- (c) (3 points) What is the decimal value of this 32-bit two's complement number?  
1111 1111 1111 1111 1111 1111 1111 1100  
(A) -4 (B) -8 (C) -16 (D) 4
- (d) (3 points) Suppose that Floating point instructions are improved with speedup=10. Only 20% of actual instructions are Floating Point instructions. What is the overall speedup?  
(A) 5 (B) 1.23 (C) 1.67 (D) 2
- (e) (3 points) Which descriptions of RISC are true?  
(A) RISC uses a simpler instruction set compared to CISC. (B) RISC has become obsolete now. (C) RISC needs more special purpose registers than CISC. (D) MIPS computer systems belong to RISC architecture.
- (f) (3 points) Which of the followings are true about multiprocessors?  
(A) Communications among different processors cannot be achieved by centralized shared memory. (B) Distributed shared-memory scheme might result in non-uniform memory access time. (C) Multiple instruction stream multiple data stream scheme offers flexible and cost performance advantages. (D) Memory Coherency can be achieved by snooping protocols.
10. (7 points) What are the advantages and challenges of longer pipelines (larger number of stages)? What are possible solutions of the challenges?
11. (10 points) Assume that a 2-way set-associative cache contains 1024 blocks (lines) and each block has 8 bytes.
- (a) (3 points) If the address is 16 bits long, what values are the tag "bits" in the block containing the data with the address "0x8F8A"?
- (b) (3 points) Following (a), right after the data with the address 0x8F8A is accessed, what range of data addresses can be accessed in this cache, i.e. hits (because of the locality associated with 0x8F8A)? Express your answer as "0xXXXX~0xXXXX".
- (c) (4 points) Assume that the access time to this cache is 2ns and the main memory access time is 100ns, including all the miss handling. The miss rate of this cache is 5%. What is the speedup if we add a secondary cache that has a 20ns access time and the miss rate of this secondary cache is 10%?

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12. (15 points) You are designing a control unit.

(a) (3 points) For simple control designs, you choose the hardwired approach.

Given a control bit "R" with the inputs "A", "B" and "C", you have determined that R is asserted in the following four conditions:

- A=0 and C=1
- A=1 and B=1
- A=1, B=0 and C=1
- B=1 and C=1

Show your implementation by using a PLA without simplification.

(b) (3 points) Following (a), please simplify it by using Karnaugh map so that the smallest number of AND/OR gates can be used.

(c) (3 points) Following (b), you are given "NAND" gates only. Please show your design.

(d) (6 points) For other parts, you choose to adopt the microprogramming approach. Please describe briefly how you use microprogramming for the control design.

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