所別：電機工程學系碩士班 甲組(一般生) 科目：計算機組織

1. Answer the following problem briefly.
   (a) The ARM processor is a RISC or a CISC machine. (2%)
   (b) How much general purpose registers does the ARM processor have in supervisor mode? (2%)
   (c) The ARM processor supports only little-endian, only big-endian, or both little-endian and big-endian memory addressing modes. (2%)
   (d) List two key objectives which the USB (Universal Serial Bus) has been designed to meet. (4%)

2. Design an 8-bit carry select adder using 4-bit ripple carry adders and 2-input multiplexers.
   (a) Draw the block diagram of the 8-bit carry select adder using the block diagrams of 4-bit ripple carry adder and 2-input multiplexer shown in Fig. 1, and explain how the 8-bit carry select adder works. (10%)

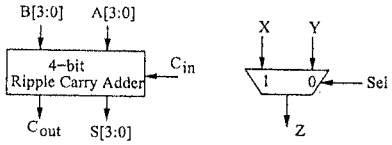

Figure 1: Block diagrams of 4-bit ripple carry adder and 2-input multiplexer.

   (b) Assume the critical delay of a 4-bit ripple carry adder and a 2-input multiplexer is 4ns and 0.2ns, respectively. Calculate the critical delay of the 8-bit carry select adder. (5%)

3. A computer system has L1 and L2 caches. The local hit rates for L1 and L2 are 90% and 80%, respectively. The miss penalties are 10 and 50 cycles, respectively. Assuming a CPI of 1.2 without any cache misses and an average of 1.1 memory accesses per instruction, (a) what is the effective CPI after cache misses are factored in? (5%) (b) Taking the two levels of caches as a single cache memory, what are its miss rate and miss penalty? (5%)

4. Figure 2 depicts a 4-stage branch prediction scheme that corresponds to keeping 2 bits of history. As long as a branch continues to be taken, we predict that it will be taken the next time (the "Predict taken" state in the Fig. 2). After the first misprediction, the state is changed, but we continue to predict that the branch will be taken. A second misprediction causes another change of state, this time to a state that causes the opposite prediction. Now a processor runs a program that consists of two nested loops, with a single branch instruction at the end of each loop and no other branch instruction anywhere. Also, the outer loop is executed 10 times and the inner loop 20 times. Determine the accuracy of the following two branch prediction strategies: (a) always predict taken, (5%) (b) use the branch prediction scheme shown in Fig. 2. (10%) (Hint: Accuracy is defined as the ratio of the number of predictions to the number of total branch predictions.)

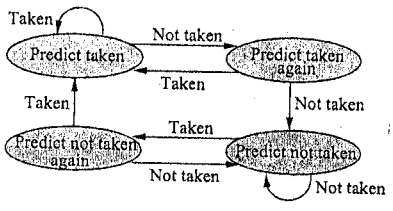

Figure 2: A 4-stage branch prediction scheme.

注意：背面有試題

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5. An example of MIPS machine assembly language notation
`op a, b, c` means an instruction with an operation `op` on the two variables `b` and `c`, and to put their result in `a`. Now a C language statement is as:
`f = (g + h) - (i + j);`
The variables `f`, `g`, `h`, `i`, and `j` can be assigned to the registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Now we use two temporary registers `$t0` and `$t1` to write the compiled MIPS assembly code as follows:

```
add     $t0,  $s1   ,  ___(A)__
__(C)__ $t1,  $s3   ,  ___(B)__
sub     $s0,  __(D)___, ___(E)__
```

Please fill the results on the blank (A), (B), (C), (D), and (E). *(10%)*

6. Please answer the following questions:
   a) Discuss the differences between "RISC" and "CISC" machine. *(6%)*
   b) A performance metric on processor is called "MOPS". What is MOPS? If a machine has the same metric on MIPS and MOPS, what does it means? *(6%)*
   c) What is floating-point format? What is the difference between floating-point and fixed-point format? *(6%)*

7. Consider two different implementations, M1 and M2, of the same instruction set. There are four classes of instruction (A, B, C, and D) in the instruction set. M1 has a clock rate of 500 MHz and M2 has a clock rate of 750 MHz.

Instruction class	CPI (Machine M1)	CPI (Machine M2)
A	1	2
B	2	2
C	3	4
D	4	4

(hint: CPI means clock cycles per instruction)
   (1) Assume the peak performance is defined as the fastest rate that a machine can execute an instruction sequence chosen to maximum that rate. What are the peak performances of M1 and M2? Please express as instructions per second? *(6%)*
   (2) If the number of instructions executed in a certain program is divided equally among the classes of instructions. How much faster is M2 than M1? *(4%)*

8. We want to design a 6-bit carry-lookahead adder, and the fan-in of every gate must be equal to or less than 3 (Fan-in$\leq$3). Please complete the following design:
   (1) Write the expression of Carry_out (C5). *(3%)*
   (2) Draw the block diagram of the design with minimum number of logic gates. *(3%)*
   (3) Compute the delay of this deisgn. *(6%)*