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國立中央大學94學年度碩士班考試入學試題卷　共 2 頁 第 1 頁

所別：電機工程學系碩士班 甲組　科目：電子學

1. 選擇題(10 分)

Consider the circuits (a), (b), (c), and (d) shown in Fig.1, assume that every transistor is biased in the forward-active mode and has the same $\beta_F = 100$, $V_{BE(on)} = 0.7$ V, and $V_A = \infty$. If the current sources I_1, I_2, I_3, and I_4 are adjusted such that each Q_1 transistor has the same dc collector current and hence, the same small-signal parameters.

1-1 Consider the input resistance R_i, (A) which circuit has the largest input resistance?(2 分) (B)Which has the lowest input resistance? (3 分)

1-2 Consider the voltage gain $A_v = |V_{out}/V_{in}|$, (A)which circuit has the largest voltage gain?(2 分) (B)Which has the lowest voltage gain?(3 分)

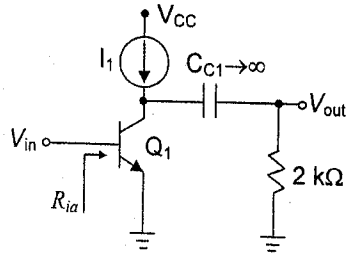

Fig. 1(a)

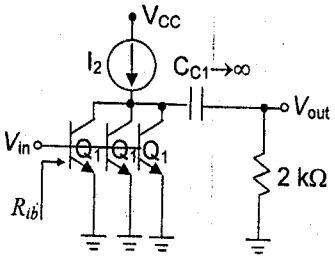

Fig. 1(b)

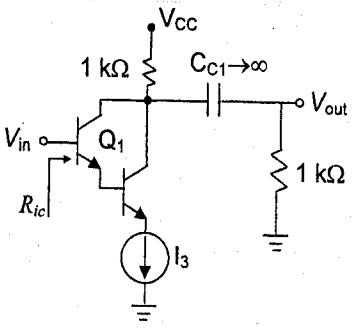

Fig. 1(c)

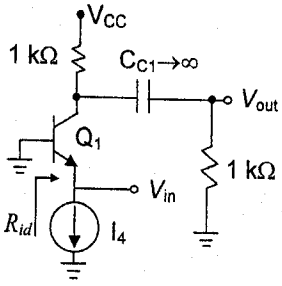

Fig. 1(d)

2. 選擇題(20 分)

For the cascode amplifier as shown in Fig. 2, let Q_1 and Q_2 be identical with $V_t = 0.6$ V, $\mu_n C_{ox} = 160$ μA/V^2, $\lambda = 0.05$ V^{-1}, $\chi = 0.2$, W/L = 100, and $V_{OV} = 0.2$ V.

2-1 (4 分) What must the bias current I can be ? (A) 32 μA, (B) 54 μA, (C) 108 μA, (D) 160 μA, (E) 320 μA.

2-2 (4 分) Find the open circuit voltage gain A_{V0}. (A) 200 V/V, (B) 241 V/V, (C) 4820 V/V, (D) 48200 V/V, (E) 441 V/V.

2-3 (4 分) Calculate the value of the effective short-circuit transconductance, Gm, of the cascode amplifier. (A) 3.2 mA/V, (B) 1.6 mA/V, (C) 6.4 mA/V, (D) 8.0 mA/V, (E) 9.6 mA/V.

2-4 (4 分) Find the output resistance R_{out} of the amplifier (A) 62.5 kΩ, (B) 125 kΩ, (C) 320 kΩ, (D) 2.4 MΩ, (E) 15.125 MΩ.

2-5 (4 分) Ignoring the small signal swing at the input and at the drain of Q_1, find the lowest value that V_{BIAS} should have in order to operate Q_1 and Q_2 in saturation. (A) 0.6 V, (B) 1.0 V, (C) 1.25 V, (D) 1.8 V, (E) 2.2 V.

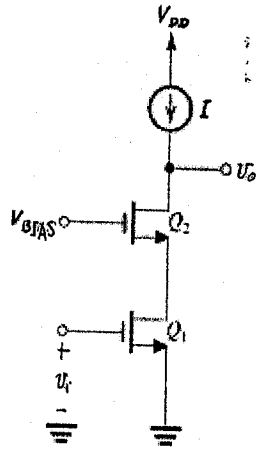

Fig. 2 The MOS cascode amplifier.

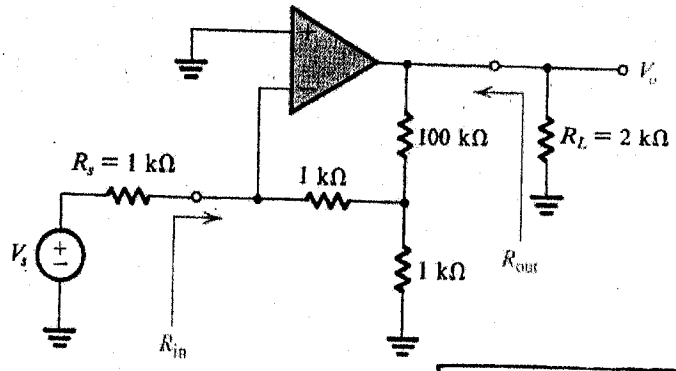

Fig. 3 Circuit for Problem 3.

注意：背面有試題

3. 選擇題(20 分)

A feedback circuit is shown in Fig. 3, the OP amp has open-loop gain $\mu = 10^4$ V/V, $R_{id} = 100$ kΩ, and $r_o = 1$ kΩ. Use the feedback analysis.

3-1 (5 分) Identify the feedback topology to be used. (A) Shunt-Series, (B) Series-Series, (C) Shunt-Shunt, (D) Series-Shunt.

3-2 (5 分) Find the voltage gain (V_o/V_s). (A) –96 V/V, (B) –192 V/V, (C) –48 V/V, (D) –108 V/V, (E) -288 V/V.

3-3 (5 分) Find the input resistance R_{in}. (A) 15 Ω, (B) 29.9 Ω, (C) 60 Ω, (D) 1.23 kΩ, (E) 108 kΩ.

3-4 (5 分) Find the output resistance R_{out}. (A) 29.5 Ω, (B) 60 Ω, (C)120 Ω, (D) 1.23 kΩ, (E) 160 kΩ.

4. (13 分)

4-1 (10 分) Sketch the pseudo-NMOS logic circuit and pass-transistor logic circuit realizations for the Exclusive-OR function.

4-2 (3 分) Which one has the DC power dissipation problem?

5. (11 分)

5-1 (6 分) Sketch a SRAM cell and a DRAM cell.

5-2 (5 分) For a DRAM cell with a capacitance of 8 fF, refresh is required within 32ms. If a signal loss on the capacitor of 0.5V can be tolerated what is the largest acceptable leakage current of the cell?

6. (10 分) For a static CMOS logic gate, the particular PMOS network is shown in Fig.4;

6-1 (5 分) Please sketch the complementary NMOS network.

6-2 (5 分) What is the logic function output of this gate?

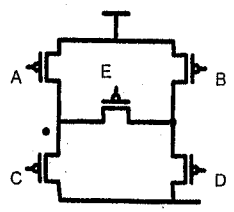

Fig. 4 Circuit for Problem 6

7. (11 分)

7-1 (6 分) Draw an N-well CMOS inverter cross-section view;

7-2 (5 分) Explain the latch-up problem briefly.

8. (5 分) Design a circuit that can be used to avoid the charge redistribution problem of the DOMINO CMOS logic gate.