國立中央大學94學年度碩士班考試入學試題卷

所別：電機工程學系碩士班 甲組　　科目：計算機組織

1. There is a program shown below. In all instructions, the destination operand is given first.

   (a) Is there any data hazard or/and instruction hazard in this program? If yes, identify the data hazard or/and instruction hazard. (5%)

   (b) Assume that the program is run at a 4-state pipelined processor with the following 4 stages: fetch, decode, execution, and write. If your answer of (a) is that the program has data hazard, we assumed the data dependency is discovered by the hardware while the instruction is being decoded. Also, the complier can handle the data hazard by inserting NOP (No-operation) instructions. Write the modified program which has been handled by the compiler. (10%)

```
Add         R1, R3, R4
Mul         R5, R4, R3
Add         R0, R2, R5
Shift_left  R1
Mul         R6, R7, R8
Mul         R9, R6, R7
```

2. A set-associative cache has 64 blocks which are divided into 4-block sets. The main memory consists of 4096 blocks, each consisting of 128 words.

   (a) How many bits are there in a main memory address? (10%)

   (b) How many bits are there in each of the WORD, SET, and TAG fields? (10%)

3. Given the bit pattern 1011 1111 0100 0000 0000 0000 0000 0000. What does it represent, assuming that it is a single precision floating point number? (Write your final answer with decimal expression.) (7%)

4. Consider the following Verilog description lines. Compare the results of variable X and Y, and the operation done in the segments (a) and (b). (8%)

```
        reg       X,Y
        initial   begin
                  X=4;
                  Y=6;
                  end
(a)     always    @(negedge clock)   begin
                  X<=Y;
                  Y<=X;
                  end
(b)     always    @(negedge clock)   begin
                  X=Y;
                  Y=X;
                  end
```

5. Explain why each of the following microprocessor features affect (or do not affect) the processing rate of the chip.

   (a). Clock frequency (3%)
   (b). Data bus width (3%)
   (c). Address bus width (3%)
   (d). Internal cache memory (3%)
   (e). Coprocessor (internal or external) (3%)

6. (a) A PC has 4 MB of RAM beginning at address 00000000H. Calculate the very last address (in hex) of this 4 MB block. (5%)

   (b) If the starting address and the ending address of the ROM block are 008000H and 010000H, calculate the size of the ROM in K. (5%)

7. (a). Decode the following ASCII code: 1010011 1110100 1100001 1110010 0110010. (2%)
   (hint: ASCII (0)=30H, ASCII (A)=41H, ASCII (a)=61H)
   (b). Write the leftmost bit selected to produce even parity of the ASCII code. (3%)

8. (a). Use the block diagram of 1-bit full adder as a basic block to construct a 32-bit ripple adder (S=A+B). (5%)
   (b). Add some logic blocks to the design of ripple adder so that it can do 2's complement subtraction (S=A-B). (5%)
   (c). Using 4-bit carry-lookahead blocks to form a 16-bit carry-lookahead adder. Draw the block diagram and write down the corresponding logic equations. (5%)
   (d). Compare the number of "gate delays" for the critical paths of two 16-bit adders, one use ripple carry and one using two-level carry lookhead. (5%)