所別：電機工程學系碩士班 甲組 科目：計算機組織

1. Machine X has a clock rate of 480 MHz and machine Y has a clock rate of 400 MHz. The following is the CPI (clock cycle per instruction) and the percentage of instructions in gcc program.

[illegible]	[illegible]	[illegible]	[illegible]
Arithmetic	2	2	48%
Data transfer	3	2	33%
Conditional branch	3	4	17%
Jump	5	4	2%

(a) Compute the CPI for gcc of machine X and Y (6%)
(b) Compute the MIPS (million instructions per second) for gcc in Machine X and Y (4%)
(c) Which machine shall be chosen to run gcc in terms of execution time? Discuss your decision (5%)

2. Exaplin the following three addressing modes used in computer. Also explain the advantages and disadvantages of using (b) and (c)
(a) Immediate addressing (4%)
(b) Base or displacement addressing (6%)
(c) PC-relative addressing (6%)

3.(a) Use the block diagram of 1-bit full adder (Fig.3a) as a basic block to construct a 16-bit ripple adder of unsigned number (S=A+B). Indicate the critical path in this design (6%)
(b) Add some logic blocks to the design of rippie adder so that it can do 2's complement substraction (S=A-B=A+(-B)) (6%)
(c) Using 4-bit carry lookahead blocks (Fig.3b) and/or other necessary logic blocks to form a 16-bit carry lookahead adder. Draw the block diagram and all necessary inputs and outputs. Indicate the critical path of the addition operation (7%)

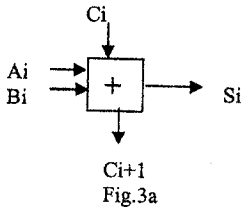

Fig.3a

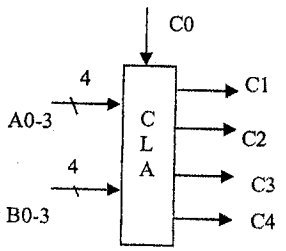

Fig.3b

$C_1 = g_0 + p_0c_0$
$C_2 = g_1 + p_1g_0 + p_1p_0c_0$
$C_3 = g_2 + p_2g_1 + p_2p_1g_0 + p_2p_1p_0c_0$
$C_4 = g_3 + p_3g_2 + p_3p_2g_1 + p_3p_2p_1g_0 + p_3p_2p_1p_0c_0$
with $gi = Ai \bullet Bi$ and pi = Ai + Bi

4.(a) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17. Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache. (8%)
(b) Using the series of references given in (1), show the hits and misses and final cache contents for a direct-mapped cache with four-word blocks and a total size of 16 words. (8%)

注意：背面有試題

參考用

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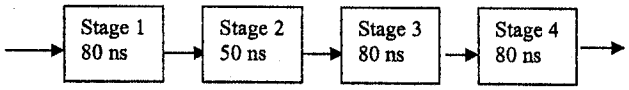
5.(a) What are the main advantages and disadvantages of pipeline? What is pipeline hazard? (8%)

(b) A pipeline machine has four stages, ie., an instruction consists of four phases (e.g., instruction fetch, instruction decode, operand fetch and execute) ; Stage 1 needs 80 nanoseconds (ns) ; Stage 2 needs 50 nanoseconds, and so on. The pipeline is shown as follows :



How much time is the pipeline machine required to complete ten instructions? (8%)

(c). How much time is the pipeline machine required to complete one hundred instructions? (8%)

6. Consider the following computer system :

-- A CPU that sustains 300 million instructions per second and average 50000 instructions in the operating system per I/O operations.

-- A memory backplane bus capable of sustaining a transfer rate of 100MB/sec.

-- SCSI-2 controllers with a transfer rate of 20MB/sec and accommodating up to seven disks.

-- Disk drives with a read/wtite bandwidth of 5MB/sec and an average seek plus rotational latency of 10ms.

If the workload consists of 64-KB reads (where the block is sequential on a track) and the user program needs 100000 instructions per I/O operation, find

(a) The maximum sustainable I/O rate. (5%)

(b) The number of disks and SCSI controllers required. Assume that the reads can always be done on an idle disk if one exists (ignore disk conflicts.) (5%)